Chapter 7. Conclusions and Future Work

7.1. Conclusions

This dissertation described the design, fabrication, and characterization of the n-AlGaAs/p-GaAs/n-GaN heterojunction bipolar transistor (HBT)[1-4], the first transistor formed via the novel technique of wafer fusion. The wafer fusion process was developed as an innovative way to combine lattice-mismatched materials for high-performance electronic devices, not otherwise obtainable via conventional all-epitaxial formation methods. Despite the many challenges of wafer fusion, successful transistors were demonstrated and improved, via optimization of both material structure and wafer fusion process conditions. Thus, this project demonstrated the integration of device materials, chosen for their optimal electronic properties, unrestricted by the conventional (and very limiting) requirement of lattice-matching.

Chapter 1 described the motivation and challenges for the wafer-fused HBT. By combining an AlGaAs-GaAs emitter-base with a GaN collector, the HBT would benefit from the high breakdown voltage of the GaN, and from the high emitter injection efficiency and low base transit time of the AlGaAs-GaAs. Because the high degree of lattice mismatch between GaAs (lattice constant of 5.65A) and GaN (3.19A) precluded an all-epitaxial formation of the HBT, the GaAs-GaN heterostructure was formed via wafer fusion. This application placed stringent demands on the electrical quality of the fused interface, as it served as the base-collector junction of an HBT. Uncontrolled bond reconstruction or residual impurities at the fused interface may have produced electronic traps or barriers, which in turn may have produced the low common-emitter current gain observed in these wafer-fused HBTs. Aside from the issue of electronic traps and barriers at the fused interface, the elevated temperature of the fusion process (500-750°C) may itself have accelerated dopant and defect diffusion, potentially degrading the sharp, thin dopant profiles required for optimal HBT electrical performance. Lower fusion temperatures would thus seem to be desirable, but for the HBT, the fusion process conditions were required to provide enough thermal energy to form a mechanically stable and electrically active fused interface. This hinted of a temperature-dependent trade-off that was further defined in Chapter 2.

As described in Chapter 2, this project began with the development of a reliable, reproducible wafer fusion process, that formed mechanically robust and electrically active GaAs-GaN heterojunctions. Additionally, during the correlation of

device electrical performance with a systematic variation of the fusion conditions over a wide range (500-750°C, 0.5-2 hours), a mid-range fusion temperature was found to induce optimal HBT performance. This discovery was further understood with high-resolution transmission electron microscopy (HRTEM) and secondary ion mass spectrometry (SIMS) analyses, which were used to assess possible reasons for variations observed in device electrical performance. By correlating the fusion process conditions with the electrical (I-V), structural (TEM), and chemical (SIMS) quality of the resulting fused interfaces, we explored the trade-off between increased interfacial disorder at low temperature (Figure 2.7) and enhanced diffusion at high temperature (Figure 3.5). Chapters 3-6 provided details of the studies outlined in Chapter 2.

Chapter 3 described the simple bi-layer structures formed via fusion: the n-GaAs/n-GaN heterostructure and the p-GaAs/n-GaN diode. I-V characteristics alone suggested that elevated fusion times and temperatures induced more optimal device electrical performance: after fusion at higher temperatures and times (750°C for 1-2 hours), n-n structures produced more linear, ohmic I-V data, and p-n diodes exhibited better breakdown characteristics and lower ideality factors (n). For example, for Be-doped diodes formed via fusion for 1 hour, n=1.4 for a fusion temperature (T_f) of 750°C, n=1.5 for T_f=700°C, and n=1.7 for T_f=650°C. However, SIMS data (Figure 3.5) revealed substantial inter-diffusion of dopants and contaminants, especially with elevated process times and temperatures. These observations began to define the trade-off between the enhanced diffusion induced

by high fusion temperatures, and the poor electrical performance induced by low fusion temperatures (likely associated with the increased interfacial disorder shown in Figure 2.7).

In Chapter 4, fusion temperatures as low as 500-550°C were used to produce HBTs with mechanically stable and electrically active fused interfaces. Due to the temperature-dependent trade-off explored in Chapters 3-4, mid-range fusion temperatures (600-650°C) induced the best dc device results. An HBT, formed via fusion at 600°C for one hour (Figure 4.4.b), exhibited a dc collector output current of $I_C \sim 1.2$ kA/cm^2 and a dc common-emitter current gain of $\beta \sim 1.2$, at V_{CE}=40V and I_B=10mA. This result was remarkable, given the challenges of GaAs-GaN wafer fusion, discussed in detail in Chapter 1. Regardless of fusion process conditions, I_C and β were consistently low, and it was important to understand the major limitations of the output current. Two likely causes were hydrogen passivation of the base dopant, carbon, and current blocking at the wafer-fused base-collector junction. In Chapters 4-6, the SIMS data exhibited large concentrations of hydrogen at the fused interface, and the I-V data of fused diodes showed an additional series resistance that may have been caused by an increase in base resistance. To ascertain if hydrogen passivation is indeed increasing the base resistance and limiting the HBT output current, samples are presently being prepared (by S. Estrada and K. McGroddy) for base resistance studies. Additionally, the ΔE_C of +0.4eV at the fused base-collector junction (estimated in Section 2.3) was likely to induce a collector current blocking effect, hence reducing β. Current blocking was also suggested by the increase of

β with increasing V_{CE} (Figure 4.6.a-c). To study and mitigate the possibility of current blocking, a base-collector setback layer was added to the HBT structure, as described in Chapter 5.

In Chapter 5, a variety of HBT designs were tested and the electrical performance was observed to vary with both the base-collector design and the fusion process temperature, as summarized in Table 2.1. The band diagrams of Figure 5.1 suggested that the presence of the setback layer should shift the conduction band barrier (of the fused heterojunction) into the depleted collector region. The conduction band potential would begin to drop at the base-side depletion edge of the base-collector junction, thereby providing electrons with more kinetic energy to surmount the upcoming barrier at the fused interface. Thus, the likelihood of current blocking would ideally be mitigated. The best dc device results ($I_C \sim 2.9$ kA/cm^2 and $\beta \sim 3.5$, at V_{CE}=20V and I_B=10mA) were obtained with an HBT formed via fusion at 600°C for one hour, with a 20nm p-GaAs setback layer doped with C. This was quite an improvement, as compared to an HBT without setback (described in Chapter 4), also formed via fusion at 600°C for one hour ($I_C \sim 0.83$ kA/cm^2 and $\beta \sim 0.89$, at V_{CE}=20V and I_B=10mA). However, the output current was still fairly low, perhaps due to hydrogen passivation of the base dopant, carbon.

Chapter 6 described a comparison of epitaxially grown, annealed, and wafer-fused AlGaAs-GaAs-GaAs HBTs. This study assessed the effects of fusion, and of high temperature alone (without the presence of a fused interface), on the electrical performance of the epitaxially grown HBT. The current gain, β, was highest for the

as-grown HBT (β=48, at I_B=0.6mA and V_{CE}=2V). β decreased by an order of magnitude for the sample annealed at 750°C for one hour (β=6.1). β decreased by yet another order of magnitude for the samples fused at 600-750°C for one hour (β=0.68, 0.32). As discussed in Section 6.4, this trend was likely due to diffusion effects. Both annealing and fusion were high-temperature, one-hour processes that ultimately degraded electrical performance. However, as observed with InP-GaAs fused junctions, defect-assisted diffusion was shown to exacerbate degradation in fused samples, as compared to annealed samples.[5]

Finally, fused AlGaAs-GaAs-GaAs HBTs were compared to fused AlGaAs-GaAs-GaN HBTs, demonstrating that the use of a wider bandgap collector ($E_{g,GaN} > E_{g,GaAs}$) did indeed improve HBT performance at high applied voltages, as desired for high-power applications. Given the same I_B (10mA) and the same fusion process conditions (600°C for one hour), the AlGaAs-GaAs-GaN HBT was operable to a high V_{CE} of 40V (Figure 6.6.b.i), while the AlGaAs-GaAs-GaAs HBT exhibited much more leakage when operated to a V_{CE} of only 5V (Figure 6.6.a.i).

Throughout the course of developing the AlGaAs-GaAs-GaN fused HBT, this dissertation study made a great deal of progress in understanding the critical process parameters that will ensure reliable, reproducible mechanical robustness of the fused structures. Although there is much remaining work needed to fully understand the details of the fusion process and its effects on device electrical performance, these experiments provided much insight into the applicability of wafer

fusion for electronically active, lattice-mismatched heterodevices, especially involving GaN.

7.2. Suggestions for Future Work

7.2.1. Base Resistance Studies

All our fused HBTs demonstrated low output current (up to 2.9 kA/cm^2, at V_{CE}=20V and I_B=10mA) and low current gain (up to 3.5, also at V_{CE}=20V and I_B=10mA). In Chapters 4-6, the SIMS data exhibited large concentrations of hydrogen at the fused interface, and the I-V data of fused diodes showed an additional series resistance that may have been caused by an increase in base resistance. To ascertain if hydrogen passivation is indeed increasing the base resistance and limiting the HBT output current, samples are presently being prepared (by S. Estrada and K. McGroddy) for base resistance studies. If hydrogen passivation is found to be the major limitation on HBT output current and current gain, perhaps the C base dopant should replaced by another species, such as Be, which is not passivated by H. However, Be is known to diffuse more readily than C, which would be highly undesirable for HBTs exposed to the high temperatures of the fusion process.

7.2.2. Pre-fusion Surface Preparation and Analysis

As discussed in Section 2.2,the basic process for pre-fusion surface preparation was established by D. Babic [6], N. Margalit [7], K.A. Black [8], and other former graduate students advised by Professors Evelyn Hu and John Bowers in the Materials and Electrical and Computer Engineering Departments at the University of California at Santa Barbara. The basic process, as designed for GaAs-InP fusion for vertical-cavity lasers, is detailed in Table 2.2. This process has not been well characterized and optimized, and leaves much room for improvement. Ideally, surface preparation would be done in an oxygen-free ambient, in order to minimize residual surface oxides that would ultimately contaminate the fused interface. Also, surface preparation would ideally be optimized by analysis (e.g. Auger) of the surface after each process step, in order to ensure minimization of surface oxides and contaminants such as photoresist residue. I-V data (Figure 2.2) revealed that electrical performance did improve with additional surface preparation. Thus, because the escape channels and oxidation processes (steps 2 and 5-7 of Table 2.2) were not included in the pre-fusion surface preparation of the HBTs described in this dissertation, this work has much potential for further improvement, with improved pre-fusion surface preparation.

7.2.3. Fusion of (111) GaAs to (111) GaN

GaAs and GaN are mismatched not only in lattice constant, but in crystal structure as well. GaAs is of the zinc blende structure, whereas GaN is of the

wurtzite structure. Along the (111) axis, the two structures differ only in stacking sequence: zinc blende stacks in an ABCABC pattern, whereas wurtzite stacks as ABAB. Thus, the most ideally bonded interface may result if both GaAs and GaN are fused along the (111) direction. It has been observed that relative wafer misalignment degrades electrical conduction through n-InGaP/n-GaP fused interfaces [9]; however, ultimately a more ideal crystallographic orientation may not enhance GaAs-GaN device performance, which may instead be limited by surface contamination and electrically active interface states (Figure 2.7).[10]

7.2.4. Optimization of the Base-Collector Design

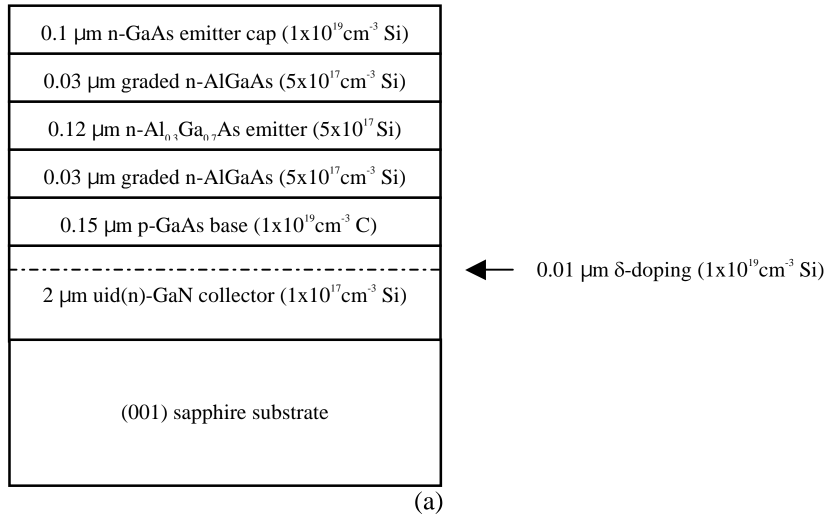
In Chapter 5, a base-collector setback layer was introduced, in order to mitigate the current-blocking effects of the conduction band barrier associated with the fused heterojunction. Alternative solutions may also be implemented, such as the addition of a Si δ-doped layer at the collector side of the fused junction (Figure 7.1), or the use of a higher band-gap setback material such as AlGaAs (Figure 7.2). By shifting the conduction band barrier to the high-field region of the energy band diagram, these potential new device structures may increase collector current and hence current gain.

However, as demonstrated with the n-GaAs setback structures (Chapter 5), the implementation of new material designs may be complicated by the issue of defect-assisted diffusion during the high-temperature fusion process. In the case of a Si δ-doped layer at the collector side of the fused junction, Si may diffuse across the

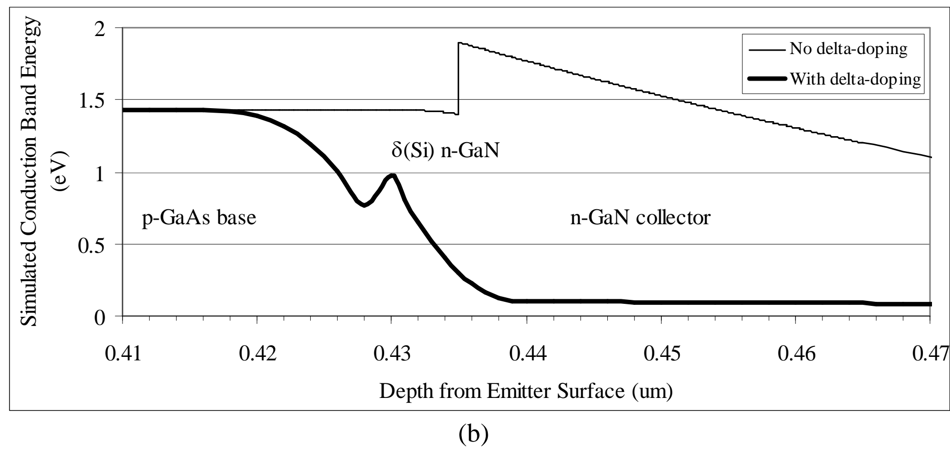
fused junction toward the p-GaAs base, perhaps effecting the same degradation simulated in Figure 5.9. However, Si should diffuse less rapidly in the δ-doped structure than in the n-GaAs setback structure, due to the lesser diffusivity of Si in GaN than in GaAs.

7.2.5. Further Electrical Analysis of the Base-Collector Junction

In Section 2.3, a thermionic barrier of 0.4eV was estimated for the wafer-fused GaAs-GaN base-collector junction of an HBT fused at 600 ^{o}C for 1 hour. Much additional work (including capacitance-voltage measurements) would have been needed, in order to determine an accurate ΔE_C for the wafer-fused heterojunction. Additionally, it would have been interesting to assess if and how ΔE_C varied with the many fusion conditions and the many base-collector material designs studied throughout the course of this dissertation work (Table 2.1). This information, in conjunction with SIMS data, would help to assess the reasons for variations observed in the electrical performance of the various samples.



(a)

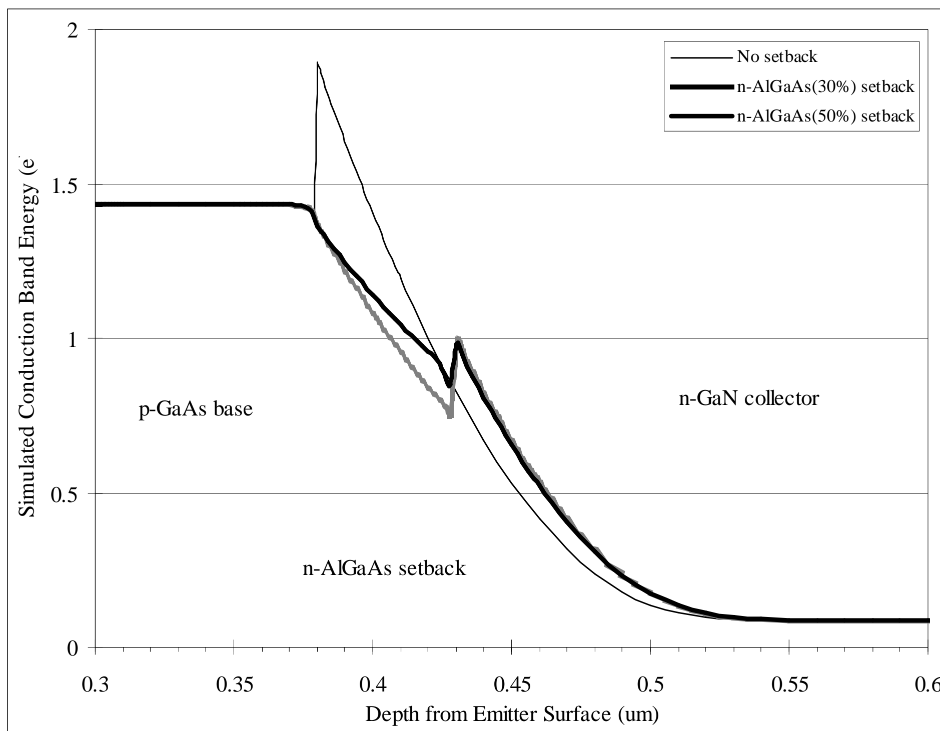


(b)

Figure 7.1. (a) Structure and (b) simulated conduction band diagram of a potential new base-collector material design, implementing a Si δ-doped layer at the collector side of the fused junction.

0.1 µm n-GaAs emitter cap ($1x10^{19}cm^{-3}$ Si)
0.03 µm graded n-AlGaAs ($5x10^{17}cm^{-3}$ Si)
0.12 µm n-$Al_{0.3}Ga_{0.7}As$ emitter ($5x10^{17}$ Si)
0.03 µm graded n-AlGaAs ($5x10^{17}cm^{-3}$ Si)
0.1 µm p-GaAs base ($1x10^{19}cm^{-3}$ C)
0.05 µm n-AlGaAs setback
2 µm uid(n)-GaN collector ($1x10^{17}cm^{-3}$ Si)
(001) sapphire substrate

(a)



(b)

Figure 7.2. (a) Structure and (b) simulated conduction band diagram of a potential new base-collector material design, implementing a base-collector setback material with a higher band gap, such as AlGaAs. The doping of the n-AlGaAs setback layer is simulated as $1x10^{17}cm^{-3}$ Si.

7.3. References

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