

Chapter 5. AlGaAs-GaAs-GaN HBT with Base-Collector Setback

5.1. Overview

This chapter describes the addition of a base-collector setback layer to the HBT design described in Chapter 4. A variety of setback structures and fusion process temperatures were examined, as summarized in Table 2.1. The best dc device results ($I_C \sim 2.9 \text{ kA/cm}^2$ and $\beta \sim 3.5$, at $V_{CE}=20\text{V}$ and $I_B=10\text{mA}$) were for an HBT formed via fusion at 600°C for one hour, with a 20nm p-GaAs setback layer doped with C. This was quite an improvement, as compared to an HBT without setback (described in Chapter 4), also formed via fusion at 600°C for one hour ($I_C \sim 0.83 \text{ kA/cm}^2$ and $\beta \sim 0.89$, at $V_{CE}=20\text{V}$ and $I_B=10\text{mA}$). Some HBTs with setback performed better than the simple HBTs (without setback); however, some setback

designs induced worse dc I-V characteristics. SIMS analysis is in progress, in order to assess possible reasons for the observed discrepancies. Although the setback layer did (in some cases) alleviate current blocking and improve output current, the output current and current gain continued to be low, perhaps due to hydrogen passivation of carbon, the base dopant (as discussed in Chapter 4).

5.2. Transistor Design

As discussed in Chapter 4, the first-generation HBT demonstrated low dc output current ($I_C \sim 0.28\text{-}1.2 \text{ kA/cm}^2$) and low current gain ($\beta \sim 0.29\text{-}4.2$). A conduction band barrier ($+\Delta E_C$) at the base-collector junction (estimated to be 0.4eV in Section 2.3) could have easily blocked the collector output current, thereby reducing β . One possible remedy was the addition of a base-collector setback layer [1], as shown in Figure 5.1. Setback layers (also called “offset” or “spacer” layers) had been incorporated into base-collector structures of InP-InGaAs-InP and InGaP-GaAs-InGaP double heterojunction bipolar transistors (DHBTs), in order to mitigate the current-blocking effects of the InGaAs-InP and GaAs-InGaP conduction band barriers.[2-6] DHBTs with setback layers demonstrated improved I-V characteristics at low V_{CE} . Figure 5.1 shows the material structures and simulated band diagrams, for fused AlGaAs-GaAs-GaN HBTs with and without a base-collector setback layer. The band diagrams suggested that the presence of the setback layer should shift the conduction band barrier (of the fused heterojunction) into the depleted collector

region. The conduction band potential would begin to drop at the base-side depletion edge of the base-collector junction, thereby providing electrons with more kinetic energy to surmount the upcoming barrier at the fused interface. Thus, the likelihood of current blocking would be alleviated.

The samples described in this chapter were fused by S. Estrada (using the procedure described in Section 2.2) and processed into I-V test structures by J. Champlain (using the procedure described in Section 2.3).

5.3. Variation of Setback Distance

Figure 5.1 shows the material structures and the simulated energy band diagrams, for HBTs with and without an n-GaAs base-collector setback layer. HBTs were formed via wafer fusion (at 600-750°C for one hour) using the process described in Section 2.2. Unlike the HBTs of Chapter 4, the HBTs described in this section included an n-GaAs base-collector setback layer, 20 or 50nm thick. It was important to investigate multiple setback layer thicknesses, as the use of a setback layer has been shown to involve a trade-off between higher breakdown voltage (with smaller setback width) and lower saturation voltage (with higher setback width).[4] A high breakdown voltage results from the wide energy bandgap of the collector material, which is wider than the bandgap of the setback material. A low saturation voltage results from the mitigation of current blocking, as induced by the presence of the setback layer.

The new HBTs introduced in this section utilized a thinner base (100nm) than did the simpler HBT structure of Chapter 4 (150nm). A thinner base was used in order to reduce the base transit time, thereby increasing the current gain. The Si doping concentration of the n-GaAs setback layer ($1 \times 10^{17} \text{ cm}^{-3} \text{ Si}$) was roughly equal to the Si concentration of the unintentionally doped (uid)-GaN collector. HBTs using other setback material dopants and doping concentrations are described later in this chapter.

Gummel plots and dc common-emitter I-V characteristics for the HBTs with setback are shown in Figures 5.2 and 5.3. For easier comparison of the various setback designs, Figures 5.4 and 5.5 show key parameters extracted from the Gummel plots and common-emitter curves. As with the simple HBTs without setback (Figures 4.5 and 4.6), a mid-range fusion temperature (650°C) resulted in the most promising I-V data. For the simple HBTs, a low fusion temperature (550°C) led to low collector output current (I_C) and low dc common-emitter current gain (β), whereas a high fusion temperature (750°C) led to dominating base-collector leakage currents. Mid-range fusion temperatures ($600\text{-}650^\circ\text{C}$) led to the highest I_C and β that were not dominated by leakage. Regardless of setback thickness, the HBTs with setback demonstrated the same trends: For the HBTs with setback, both low and high fusion temperatures (600°C and 750°C) led to low levels of I_C ($10^{-5}\text{-}10^{-1}\text{mA}$), and I_C did not saturate over a wide range of V_{CE} (0-40V). Because these current levels were similar to the base-collector leakage currents, the samples fused at 600°C and 750°C were probably not functioning HBTs. A mid-range fusion temperature (650°C) led to

better saturation of I_C vs. V_{CE} , and also higher I_C (4-7mA). As described in Chapter 4, the poor performance resulting from a low fusion temperature may have been due to the increased disorder at an interface that was fused at an insufficiently high temperature (Figure 2.7). The poor performance resulting from a high fusion temperature may have been due to increased diffusion.

In comparing the various setback designs, the data show that electrical performance degraded with increasing setback layer thickness (0-50nm). Figure 5.4 shows that the output current and the current gain both decrease with increasing setback layer thickness, whereas the base-collector leakage current increases with increasing setback layer thickness. Additionally, Gummel plots were taken at several values of V_{CB} : $V_{CB}=0$ for Figure 5.2, $V_{CB}=20V$ for Figure 5.6, and $V_{CB}=40V$ for Figure 5.7. The current gains for all these data are summarized in Figure 5.8. Because the gain increased by orders of magnitude with increasing reverse bias on the base-collector junction, this particular setback design seemed unsuccessful at mitigating the current blocking at the base-collector junction.

The poor performance of the HBTs with n-GaAs setback may have been due to diffusion effects. One possibility was that the setback layer may have become effectively p-type. In this case, the base would have effectively become wider, thereby increasing the likelihood of base recombination and the reduction of both I_C and β . Another possibility involved the diffusion of Si. Because dopant diffusion was certainly occurring in these structures at the high fusion temperatures, and because the diffusivity of Si was higher in GaAs than in GaN, it was likely that the addition

of an n-GaAs setback layer provided both an additional Si source and an additional medium through which the Si was able to diffuse toward the fused interface (which has been shown to act as a gettering site, as discussed in Section 3.4). Figure 5.9 illustrates that a more aggregated Si concentration at the fused base-collector junction can substantially alter the simulated energy band structure in a number of possible ways, potentially decreasing both I_C and β . Thus, subsequent HBT material structures were designed to address not only the conduction band spike at the fused interface, but also the issue of dopant diffusion. Section 5.4 describes the use of a decreased Si dopant concentration in the setback layer, and Section 5.5 describes the use of setback dopants expected to have lower diffusivities than Si.

5.4. Variation of Setback Doping Concentration

Figure 5.10 shows simulated conduction band diagrams for various HBT structures. An HBT without setback, as described in Chapter 4, was compared to HBTs containing an n-GaAs setback layer of either low or high Si dopant concentration. The band diagrams for the two different setback designs were nearly identical. However, these simulations did not account for additional aggregation of Si at the base-collector junction due to diffusion during the high-temperature fusion process, as discussed in Sections 3.4 and 5.3. At the same temperature, the setback material with the higher Si concentration was more susceptible to diffusion effects.

HBTs without setback were compared to HBTs with base-collector setback. The n-GaAs setback layers were 20nm thick, with either a lower Si doping of $<1 \times 10^{16} \text{cm}^{-3}$ or a higher Si doping of $1 \times 10^{17} \text{cm}^{-3}$. Figure 5.11 shows common-emitter I-V characteristics of HBTs formed via wafer fusion for one hour at 600-650°C. Figure 5.12 compares I_C and β for the various HBT designs. Figure 5.13 compares the base-collector leakage. I_C , β , and base-collector leakage were consistently higher for the HBTs fused at the lower temperature (600°C). I_C , β , and base-collector leakage exhibited less sample-to-sample variation for HBTs fused at the higher temperature (650°C). As in Section 5.3, the HBT without setback produced the highest I_C and β . Although the HBTs with setback (fused at 650°C) exhibited the same base-collector leakage current, the higher setback doping led to a higher I_C and β . The HBT with the low-doped setback exhibited lower saturation voltage than both the HBT without setback and the HBT with highly doped setback; however, this was likely due to the lower I_C demonstrated by the low-doped setback at a given I_B and V_{CE} .

5.5. Variation of Setback Dopant

Figure 5.14 shows the simulated conduction band diagrams for various HBT structures. An HBT without setback, as described in Chapter 4, was compared to HBTs containing a GaAs setback layer of either low n-type (Si) doping or low p-type (C) doping. The band diagrams for the two different setback HBTs were nearly

identical; however, these simulations did not account for additional aggregation of dopants at the base-collector junction due to diffusion during the high-temperature fusion process, as discussed in Sections 3.4 and 5.3.

Figure 5.15 shows the common-emitter I-V characteristics of HBTs formed via wafer fusion for one hour at 600-650°C. HBTs had a base-collector setback material of either undoped-GaAs, p-GaAs lightly doped with carbon, or n-GaAs lightly doped with Si. Setback layers were 20nm thick. The fused samples were processed into I-V test structures by James Champlain, at that time working for Professor Umesh Mishra at the University of California at Santa Barbara. Comparing these HBTs with setback to an HBT without setback (Figure 4.6), Figure 5.16 shows β and base-collector leakage current for the various HBT designs. All HBT structures demonstrated higher β when formed via fusion at 600°C rather than 650°C. As in Section 5.4, the structure-to-structure variation in I_C , β , and base-collector leakage was greater for HBTs fused at 600°C than for HBTs fused at 650°C. HBTs with p-GaAs and undoped-GaAs setback exhibited much larger β when fused at 600°C rather than at 650°C, but HBTs without setback and HBTs with n-GaAs setback demonstrated β that did not vary much with fusion temperature. The best dc device results ($I_C \sim 2.9 \text{ kA/cm}^2$ and $\beta \sim 3.5$, at $V_{CE}=20\text{V}$ and $I_B=10\text{mA}$) were for an HBT formed via fusion at 600°C for one hour, with a 20nm p-GaAs setback layer doped with C. This was quite an improvement, as compared to an HBT without setback (described in Chapter 4), also formed at 600°C for one hour ($I_C \sim 0.83 \text{ kA/cm}^2$ and $\beta \sim 0.89$, at $V_{CE}=20\text{V}$ and $I_B=10\text{mA}$). Some HBTs with setback performed better than

the simple HBTs (without setback); however, some setback designs induced worse dc I-V characteristics (Figure 5.15). The n-type setback layers performed the worst (exhibiting $I_C \sim 0.64 \text{ kA/cm}^2$ and $\beta \sim 0.57$, at $V_{CE}=20\text{V}$ and $I_B=10\text{mA}$) for an HBT formed via fusion at 600°C for one hour, with a 20nm n-GaAs setback layer doped with Si. Better results were obtained with unintentionally doped (“uid”) setback layers: $I_C \sim 1.7 \text{ kA/cm}^2$ and $\beta \sim 2.0$, at $V_{CE}=20\text{V}$ and $I_B=10\text{mA}$) for an HBT formed via fusion at 600°C for one hour, with a 20nm uid-GaAs setback layer. Regardless of fusion temperature, $\beta(\text{p-GaAs setback}) > \beta(\text{no setback}) > \beta(\text{n-GaAs setback})$. HBTs with p-GaAs setback exhibited higher I_C and β than HBTs without setback, as the p-GaAs setback layer diminished the effect of the conduction band barrier at the fused heterojunction. However, HBTs with n-GaAs setback exhibited lower I_C and β than HBTs without setback, probably due to defect-assisted diffusion of the Si dopant during the high-temperature fusion anneal (as discussed in Section 5.3). C and other species were also diffusing during fusion; however, Si was expected to have a particularly high diffusion constant. Additional work would have been needed, in order to fully assess the reasons for variations observed in the electrical performance of the various base-collector designs. Chapter 7 describes suggestions for future work in the analysis of these or similar wafer-fused junctions.

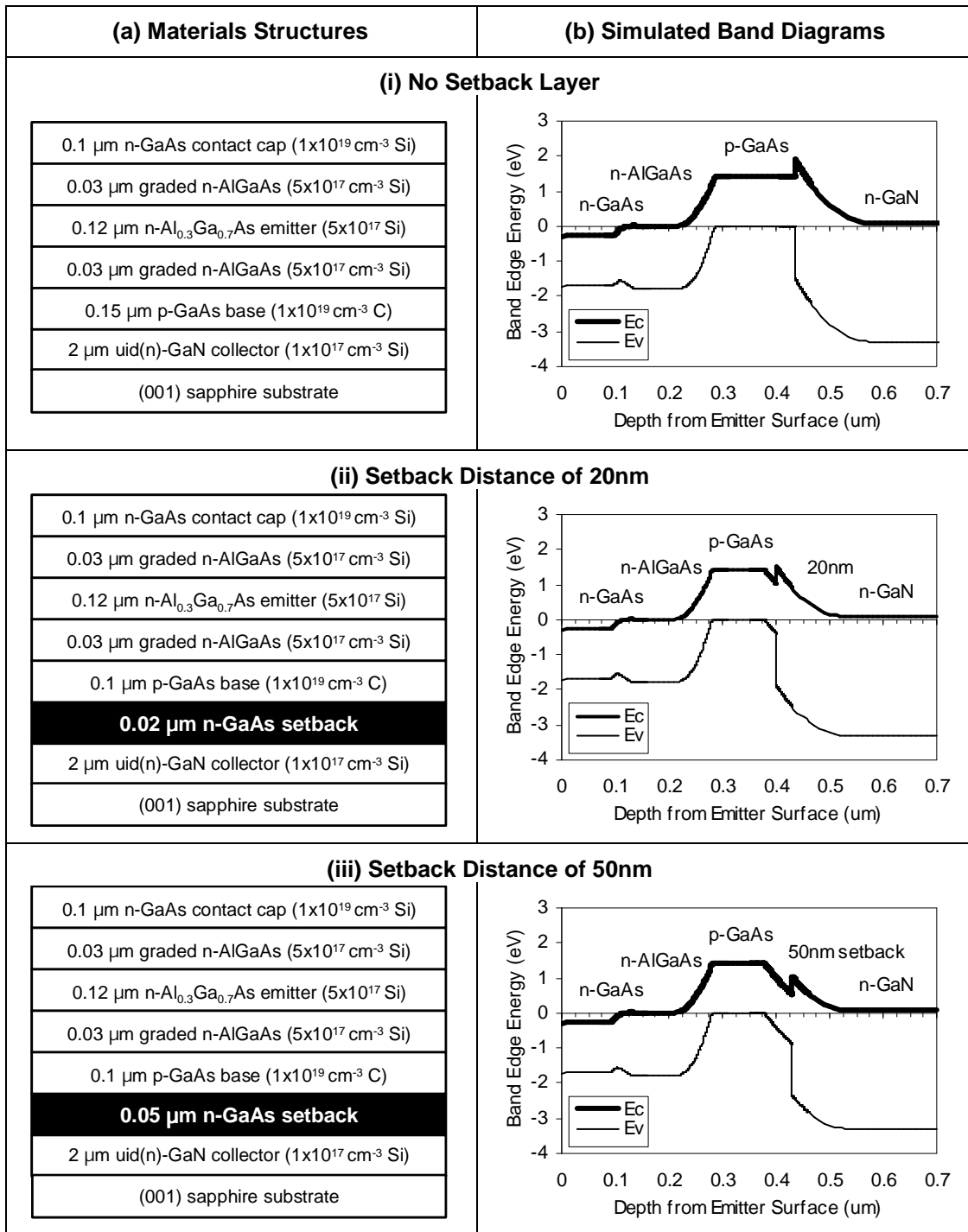


Figure 5.1. (a) Materials structures and (b) simulated energy band diagrams of HBTs (i) without an n-GaAs base-collector setback layer, as described in Chapter 4, and with a setback layer of thickness (ii) 20nm and (iii) 50nm. Simple HBTs, without setback, had a thicker base ($w_B=0.15\mu\text{m}$) than did HBTs with setback ($w_B=0.1\mu\text{m}$). Doping of the n-GaAs setback layer was $1 \times 10^{17} \text{ cm}^{-3}$ Si.

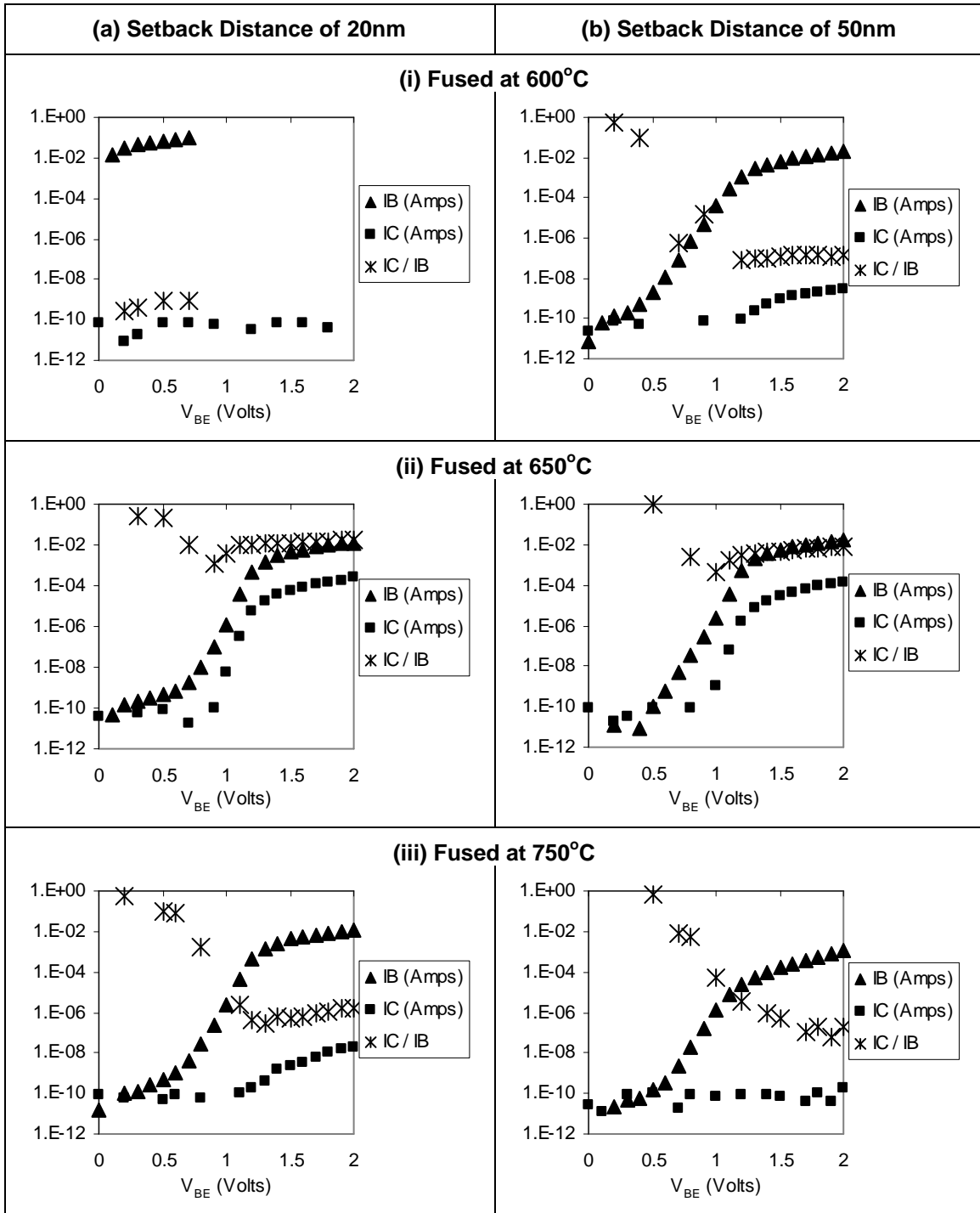


Figure 5.2. Gummel plots (with $V_{CB}=0V$) of HBTs formed via wafer fusion for one hour at (i) 600°C, (ii) 650°C, and (iii) 750°C, with an n-GaAs base-collector setback distance of (a) 20nm and (b) 50nm. Doping of the n-GaAs setback layer was $1 \times 10^{17} \text{cm}^{-3}$ Si.

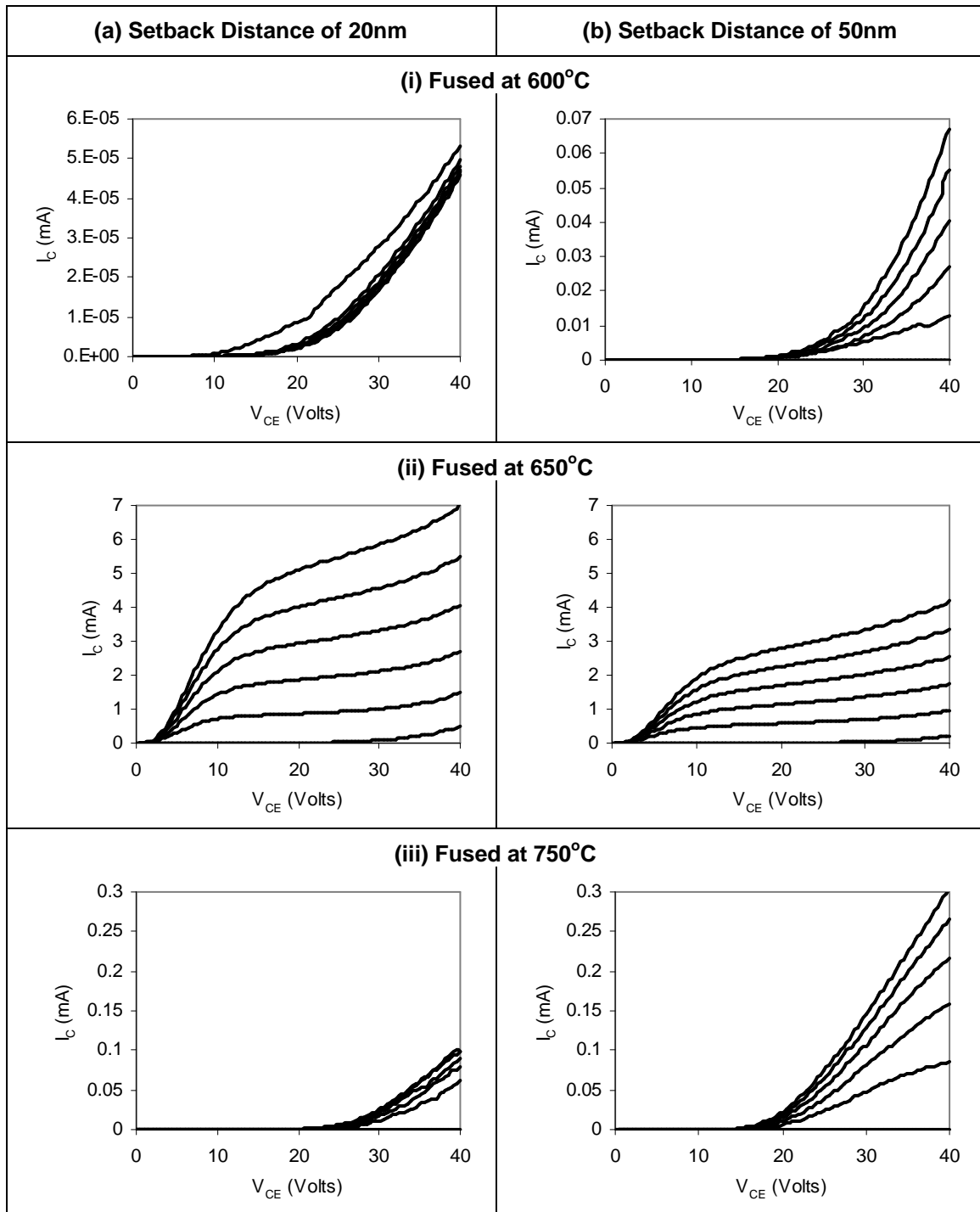


Figure 5.3. Common-emitter I-V characteristics of HBTs formed via wafer fusion for one hour at (i) 600°C, (ii) 650°C, and (iii) 750°C, with an n-GaAs base-collector setback distance of (a) 20nm and (b) 50nm. I_B step size was 2mA. Doping of the n-GaAs setback layer was $1 \times 10^{17} \text{cm}^{-3}$ Si.

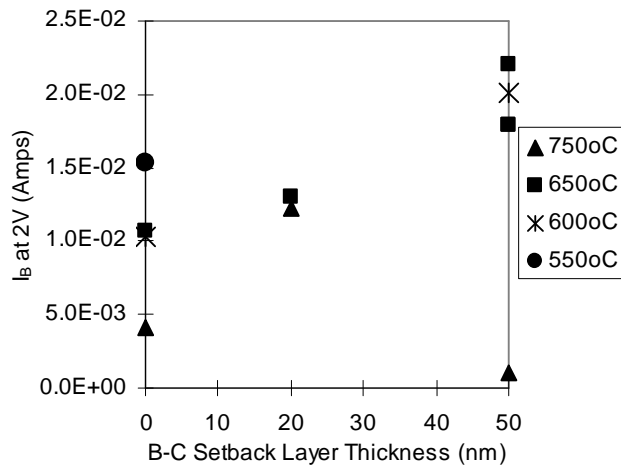


Figure 5.4.a. Gummel plot base current (I_B) of various HBT structures formed via wafer fusion at 550-750°C for one hour. The HBTs had base-collector setback distances of 0-50nm, and the base current increased with increasing fusion temperature. $V_{CB}=0V$.

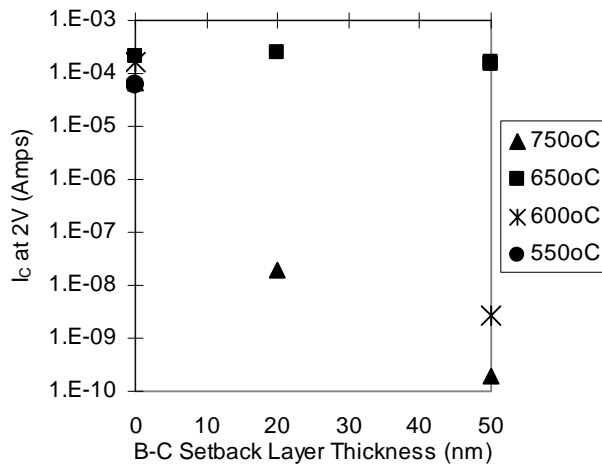


Figure 5.4.b. Gummel plot collector current (I_C) of various HBT structures formed via wafer fusion at 550-750°C for one hour. The HBTs had base-collector setback distances of 0-50nm. I_C was highest with a mid-range fusion temperature (650°C) and I_C tended to decrease with increasing setback distance. $V_{CB}=0V$.

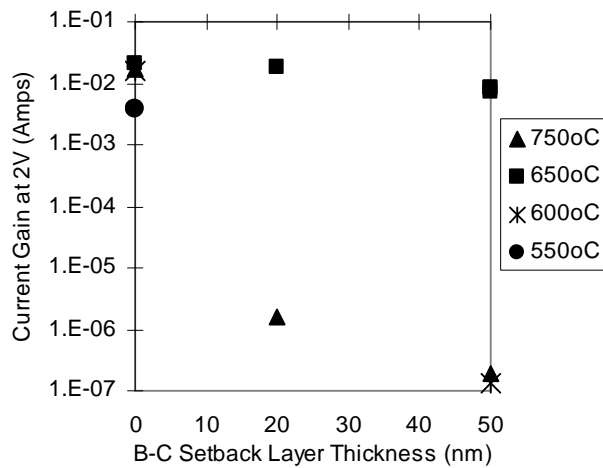


Figure 5.4.c. Gummel plot current gain (I_C/I_B) of various HBT structures formed via wafer fusion at 550-750°C for one hour. The HBTs had base-collector setback distances of 0-50nm. The gain was highest with a mid-range fusion temperature (650°C) and the gain tended to decrease with increasing setback distance. $V_{CB}=0V$.

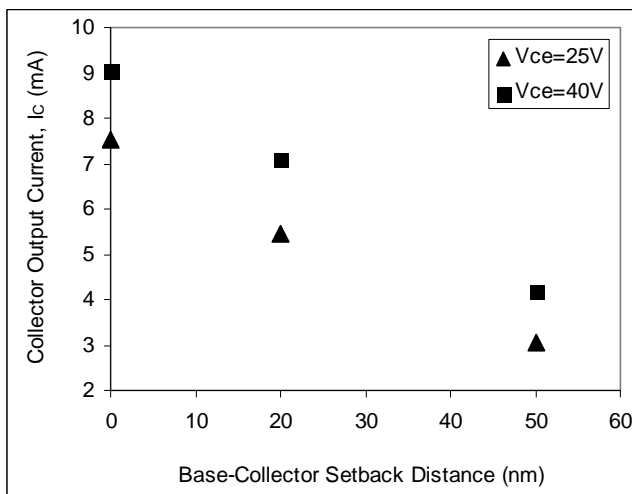


Figure 5.5.a. Common-emitter output current (I_C), at $I_B=10mA$, of various HBT structures formed via wafer fusion at $650^\circ C$ for one hour. The HBTs had base-collector setback distances of 0-50nm, and the output current decreased with increasing setback distance.

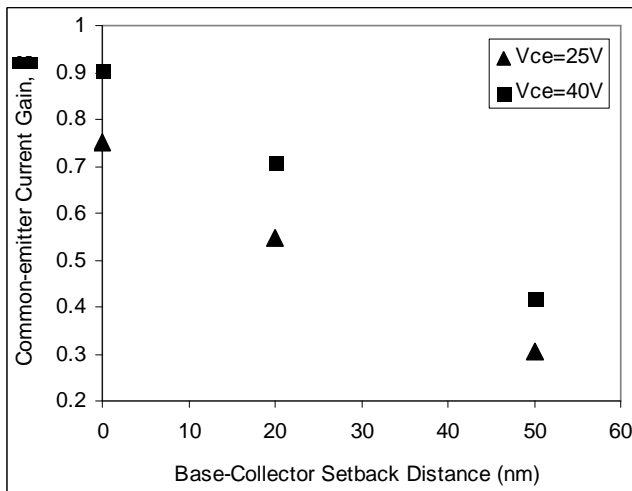


Figure 5.5.b. Common-emitter current gain (β), at $I_B=10mA$, of various HBT structures formed via wafer fusion at $650^\circ C$ for one hour. The HBTs had base-collector setback distances of 0-50nm, and the gain decreased with increasing setback distance.

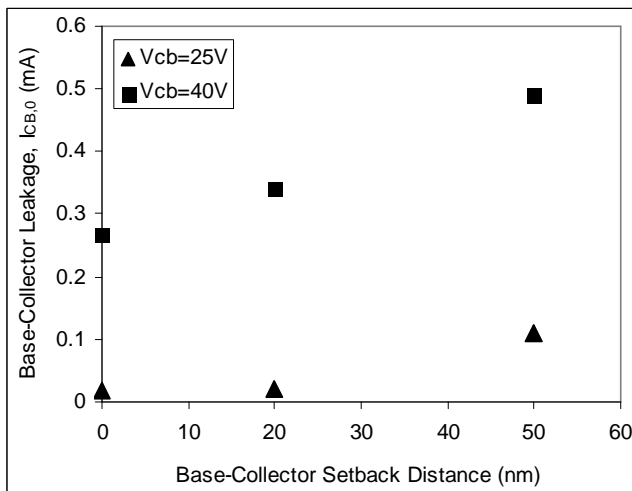


Figure 5.5.c. Base-collector leakage, measured with the emitter open, in various HBT structures formed via wafer fusion at $650^\circ C$ for one hour. The HBTs had base-collector setback distances of 0-50nm, and the leakage increased with increasing setback distance.

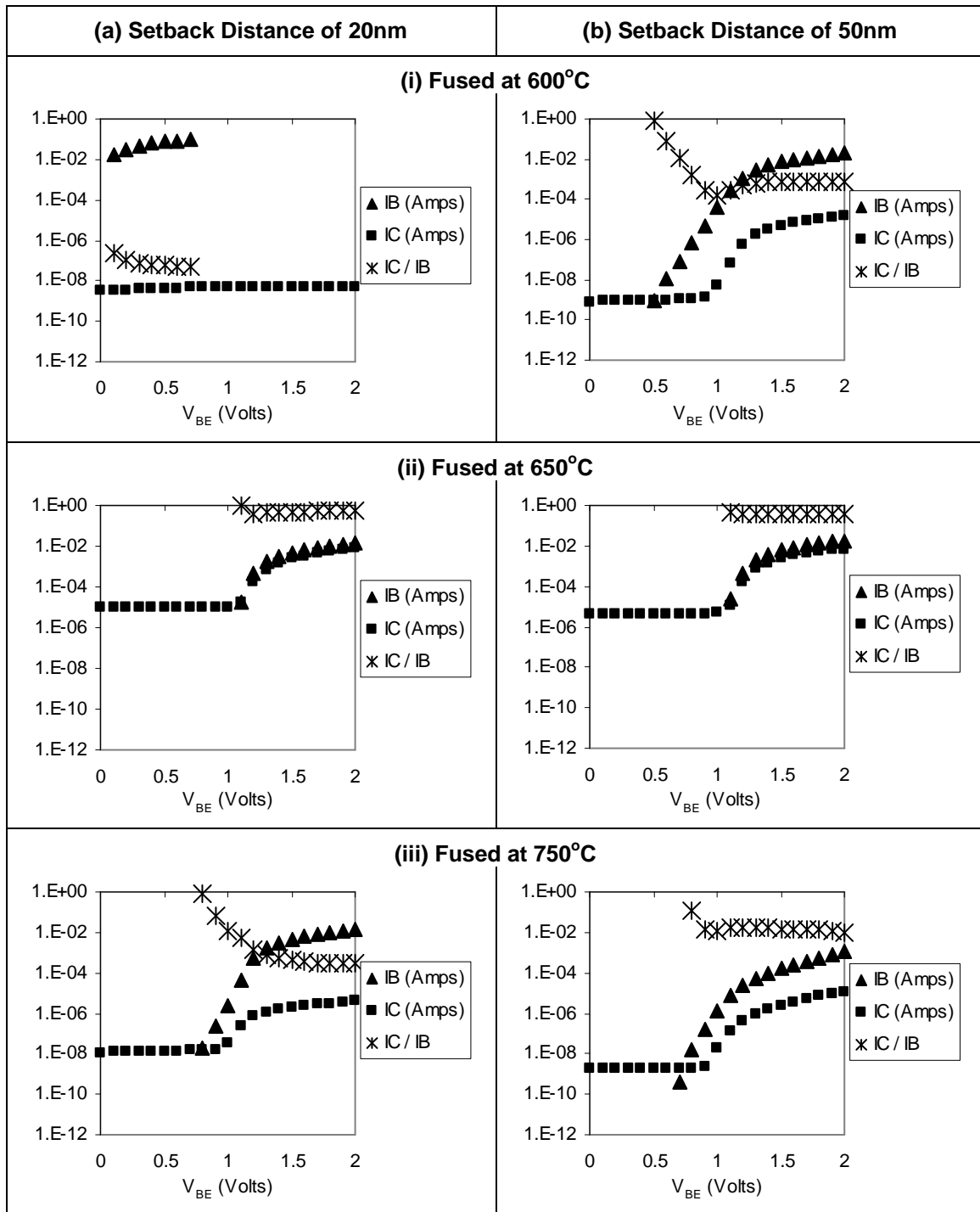


Figure 5.6. Gummel plots (with $V_{CB}=20V$) of HBTs formed via wafer fusion for one hour at (i) 600°C, (ii) 650°C, and (iii) 750°C, with an n-GaAs base-collector setback distance of (a) 20nm and (b) 50nm. Doping of the n-GaAs setback layer was $1 \times 10^{17} \text{cm}^{-3}$ Si.

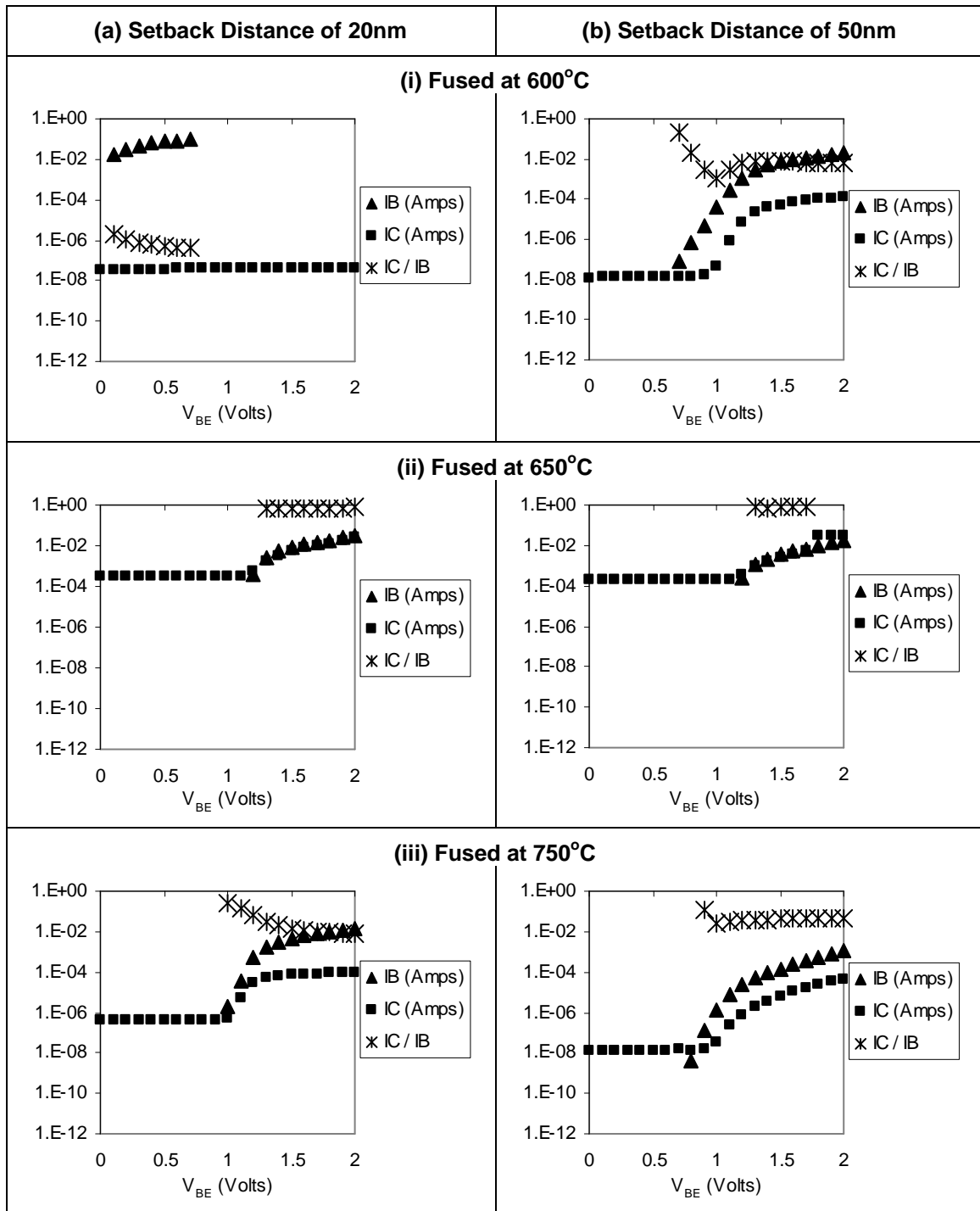


Figure 5.7. Gummel plots (with $V_{CB}=40V$) of HBTs formed via wafer fusion for one hour at (i) 600°C, (ii) 650°C, and (iii) 750°C, with an n-GaAs base-collector setback distance of (a) 20nm and (b) 50nm. Doping of the n-GaAs setback layer was $1 \times 10^{17} \text{cm}^{-3}$ Si.

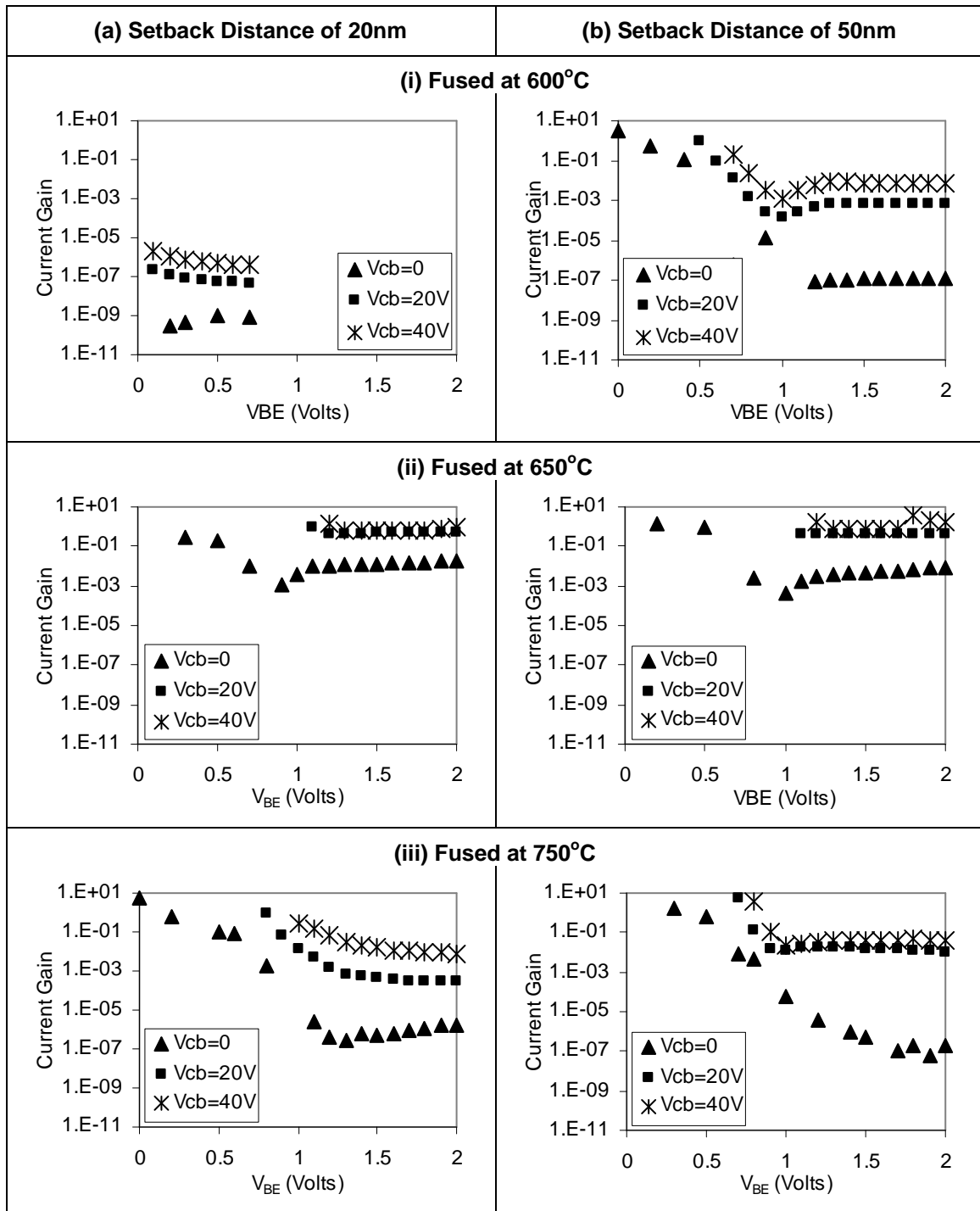


Figure 5.8. Summary of current gains from Gummel plots (with $V_{CB}=0-40V$) of HBTs formed via wafer fusion for one hour at (i) 600°C, (ii) 650°C, and (iii) 750°C, with an n-GaAs base-collector setback distance of (a) 20nm and (b) 50nm. Doping of the n-GaAs setback layer was $1 \times 10^{17} \text{ cm}^{-3} \text{ Si}$.

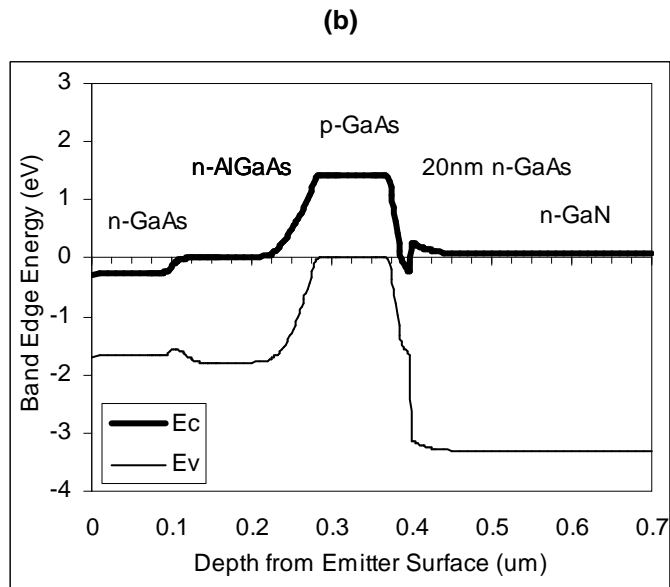
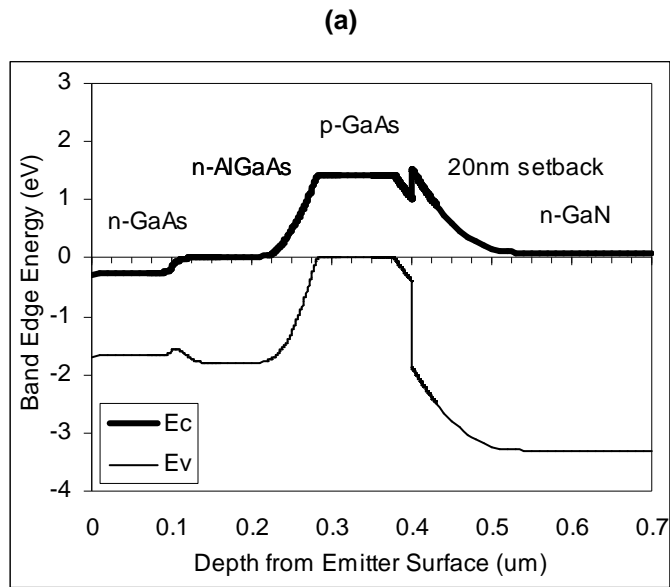


Figure 5.9. Simulated energy band diagrams of HBTs with a 20nm n-GaAs base-collector setback layer (a) assuming no Si diffusion during the fusion anneal at 600-750°C, and (b) assuming aggregation of active Si dopants at the fused interface.

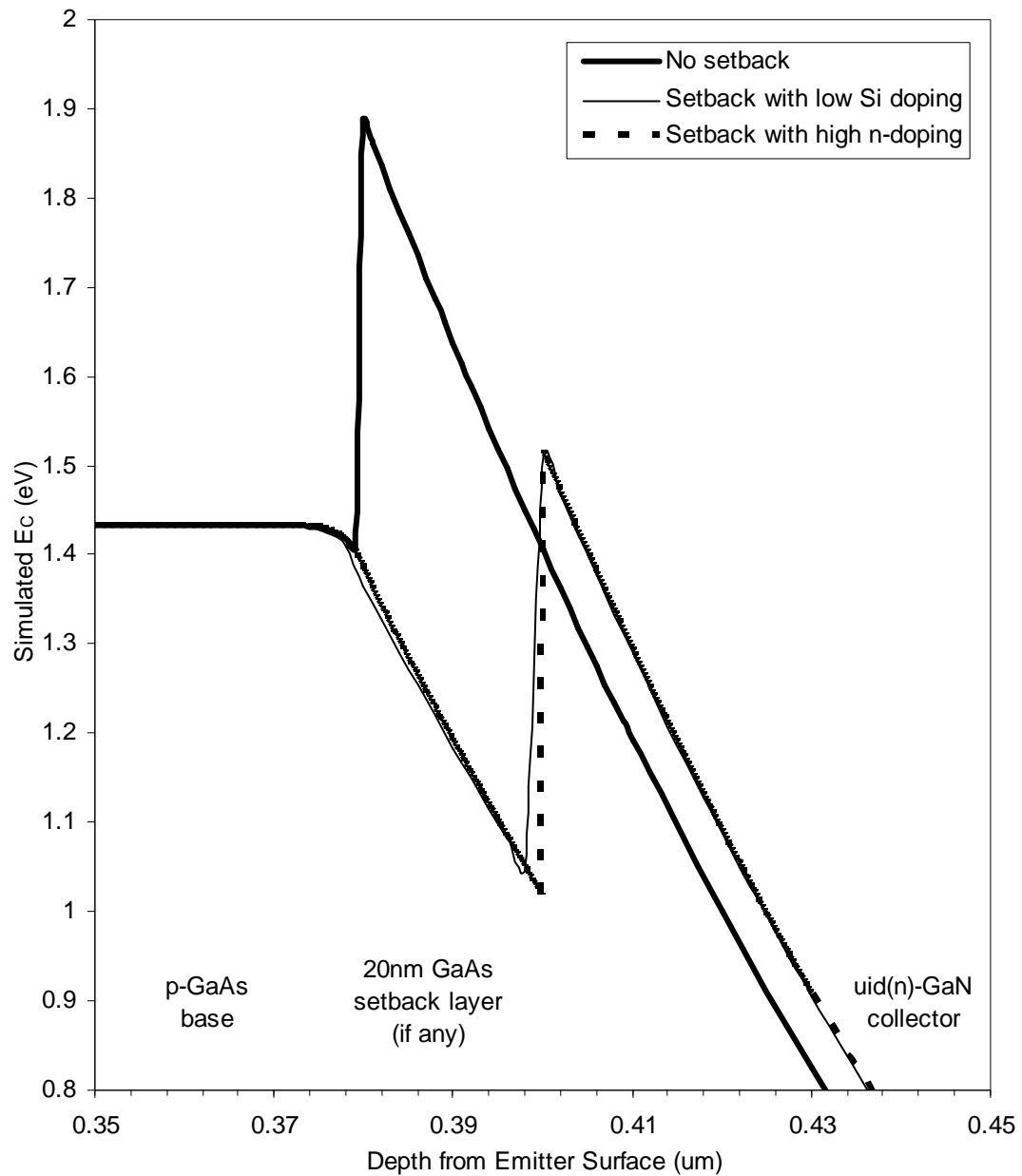


Figure 5.10. Simulated conduction band diagrams for HBTs without an n-GaAs base-collector setback layer, as described in Chapter 4, and with a setback layer of low and high Si dopant concentration. These simulations did not account for additional aggregation of Si at the base-collector junction due to diffusion during the high-temperature fusion process, as discussed in Section 3.4.

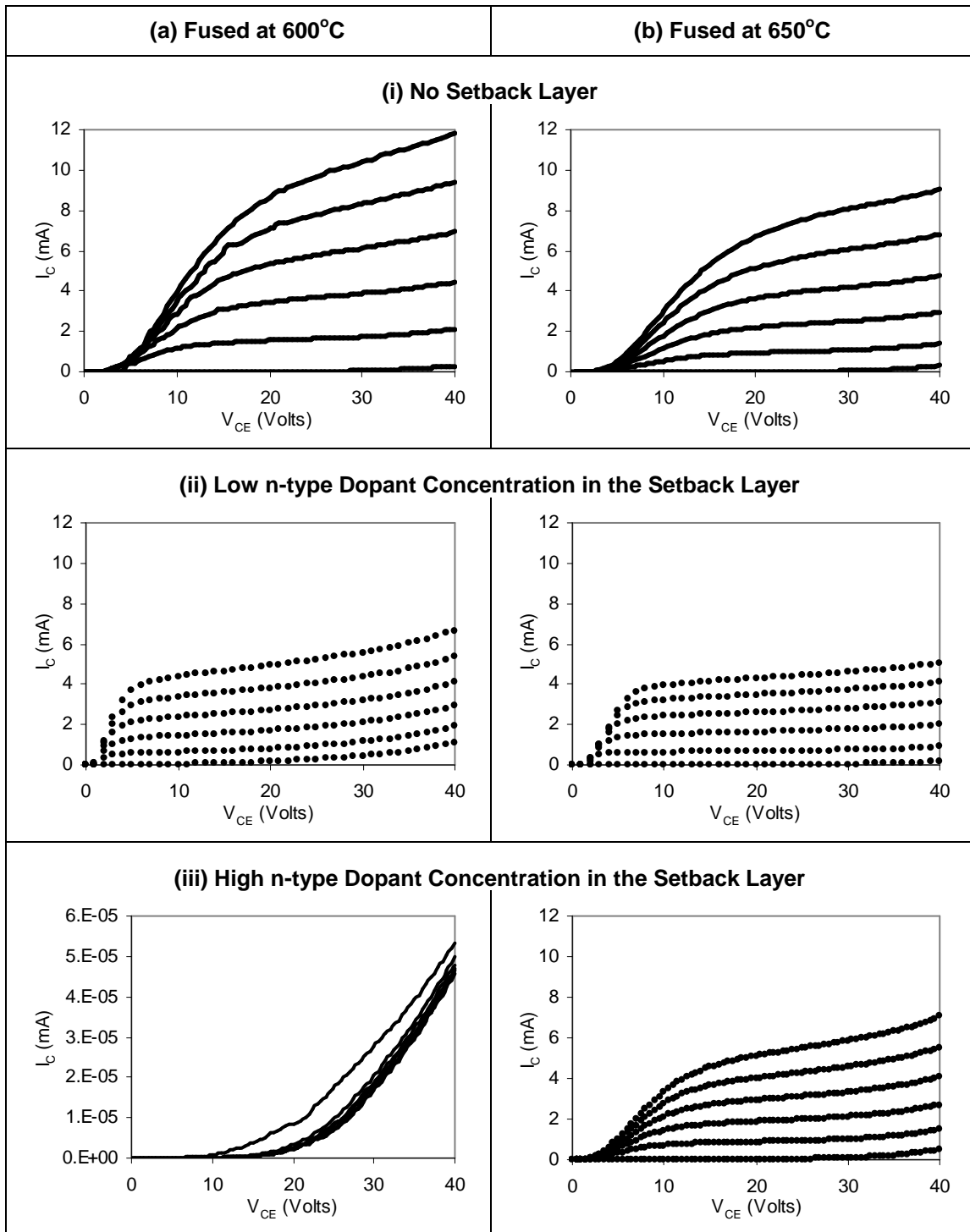


Figure 5.11. Common-emitter I-V characteristics of HBTs formed via wafer fusion for one hour at (a) 600°C and (b) 650°C. HBTs had (i) no base-collector setback layer, and an n-GaAs setback layer with (ii) low Si doping of $<1 \times 10^{16} \text{ cm}^{-3}$ and (iii) high Si doping of $1 \times 10^{17} \text{ cm}^{-3}$. Setback layers were 20nm thick. I_B step size was 2mA.

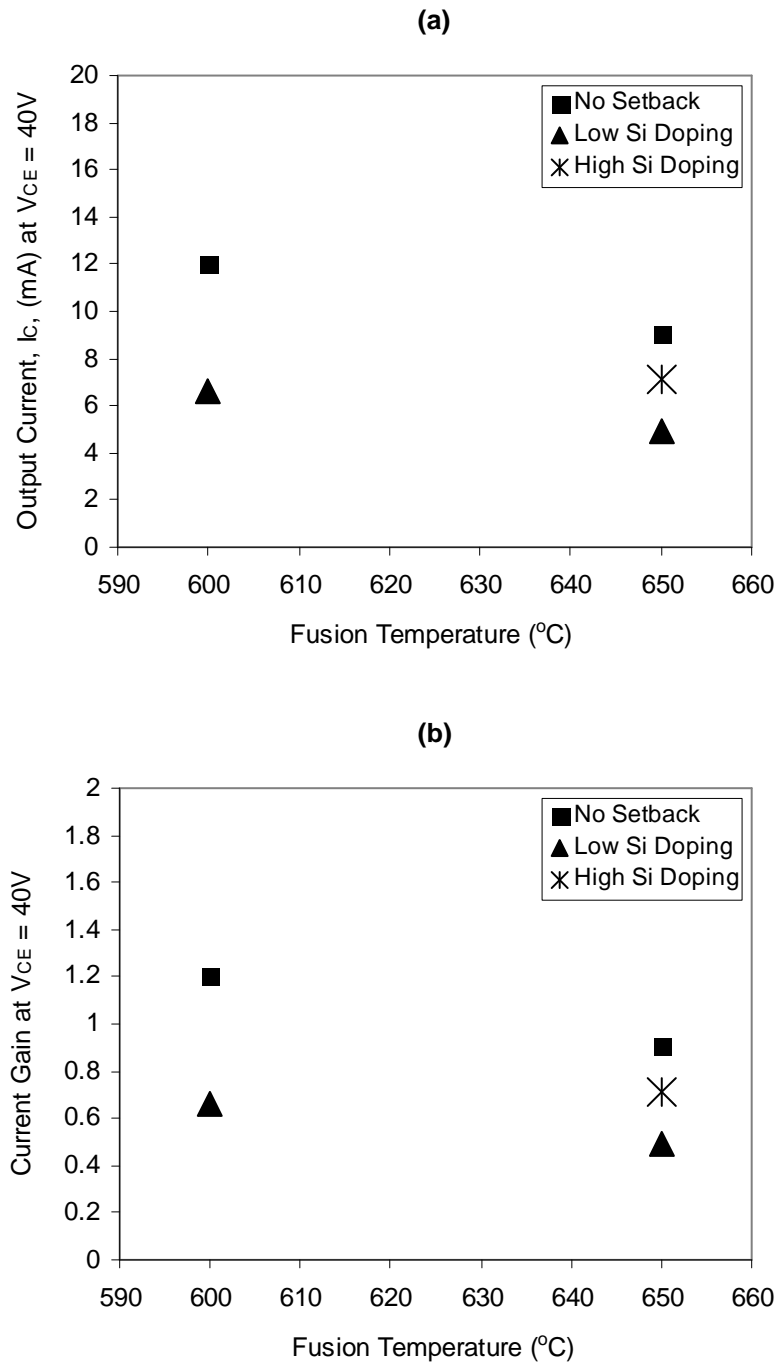


Figure 5.12. (a) Common-emitter output current, I_C , and (b) current gain, β , both at $I_B=10mA$, of various HBT structures formed via wafer fusion at 600-650°C for one hour. The HBTs had either no base-collector setback layer or an n-GaAs setback layer (20nm thick) with either a low Si dopant concentration of $<1 \times 10^{16} \text{cm}^{-3}$ or a high Si dopant concentration of $1 \times 10^{17} \text{cm}^{-3}$.

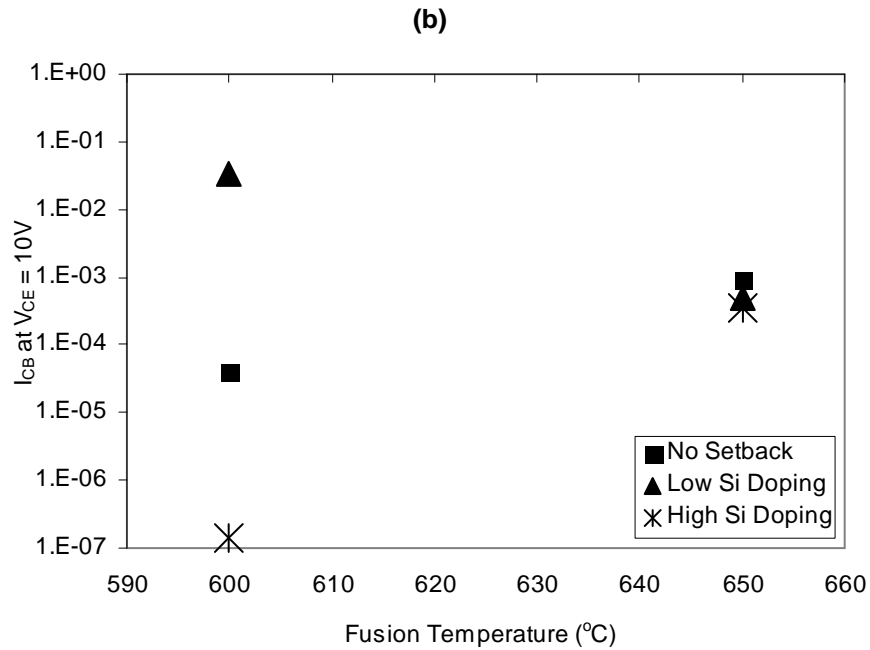
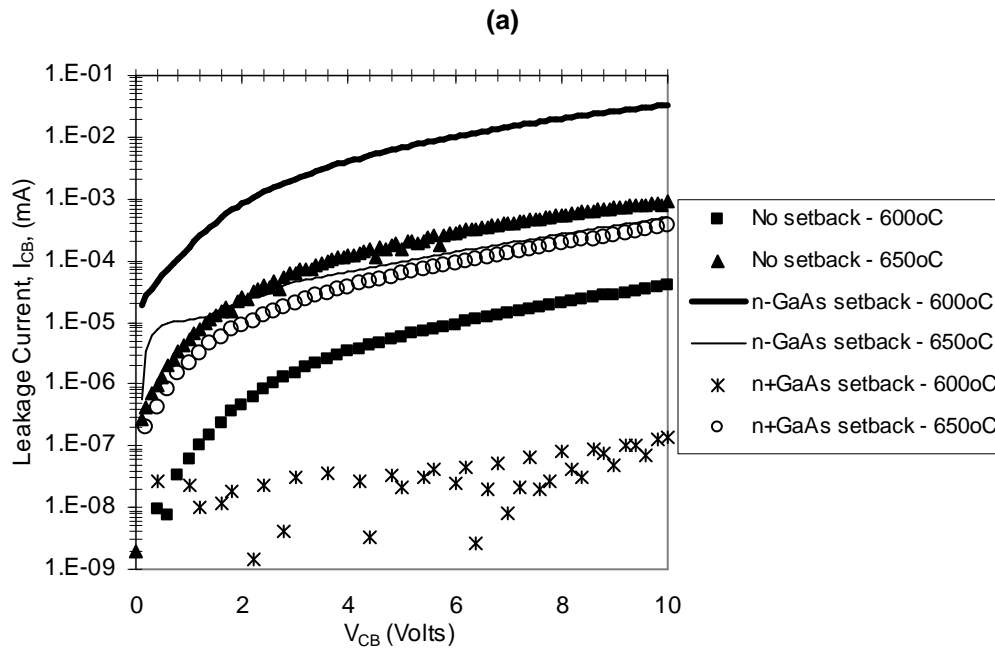


Figure 5.13. Base-collector leakage current, measured with the emitter open, in various HBT structures formed via wafer fusion at 600-650 $^{\circ}C$ for one hour. The HBTs had either no base-collector setback layer or an n-GaAs setback layer (20nm thick) with either a low Si dopant concentration of $<1 \times 10^{16} \text{cm}^{-3}$ or a high Si dopant concentration of $1 \times 10^{17} \text{cm}^{-3}$.

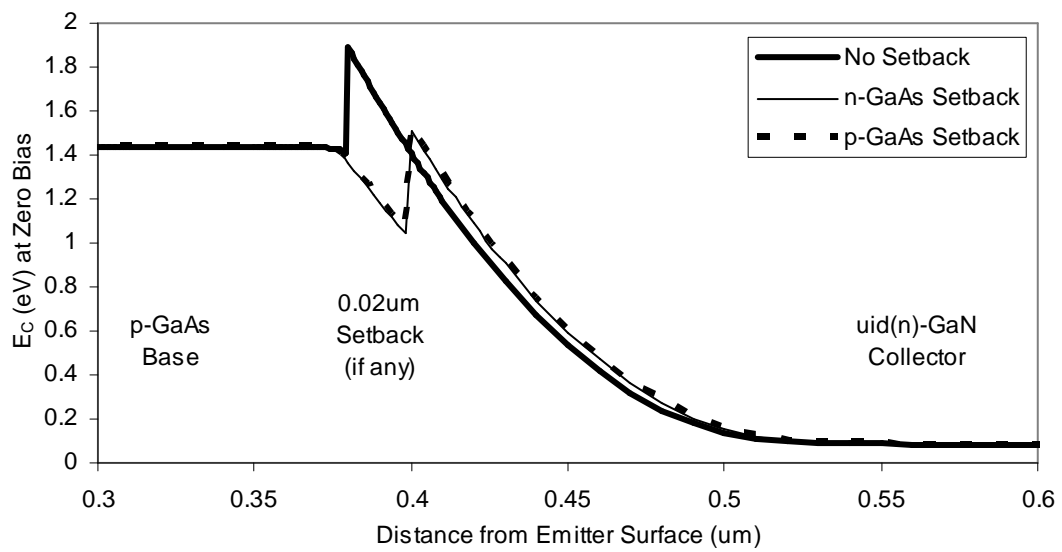


Figure 5.14. Simulated conduction band diagrams for HBTs without a GaAs base-collector setback layer, as described in Chapter 4, and with a setback layer of low n-type (Si) doping and low p-type (C) doping.

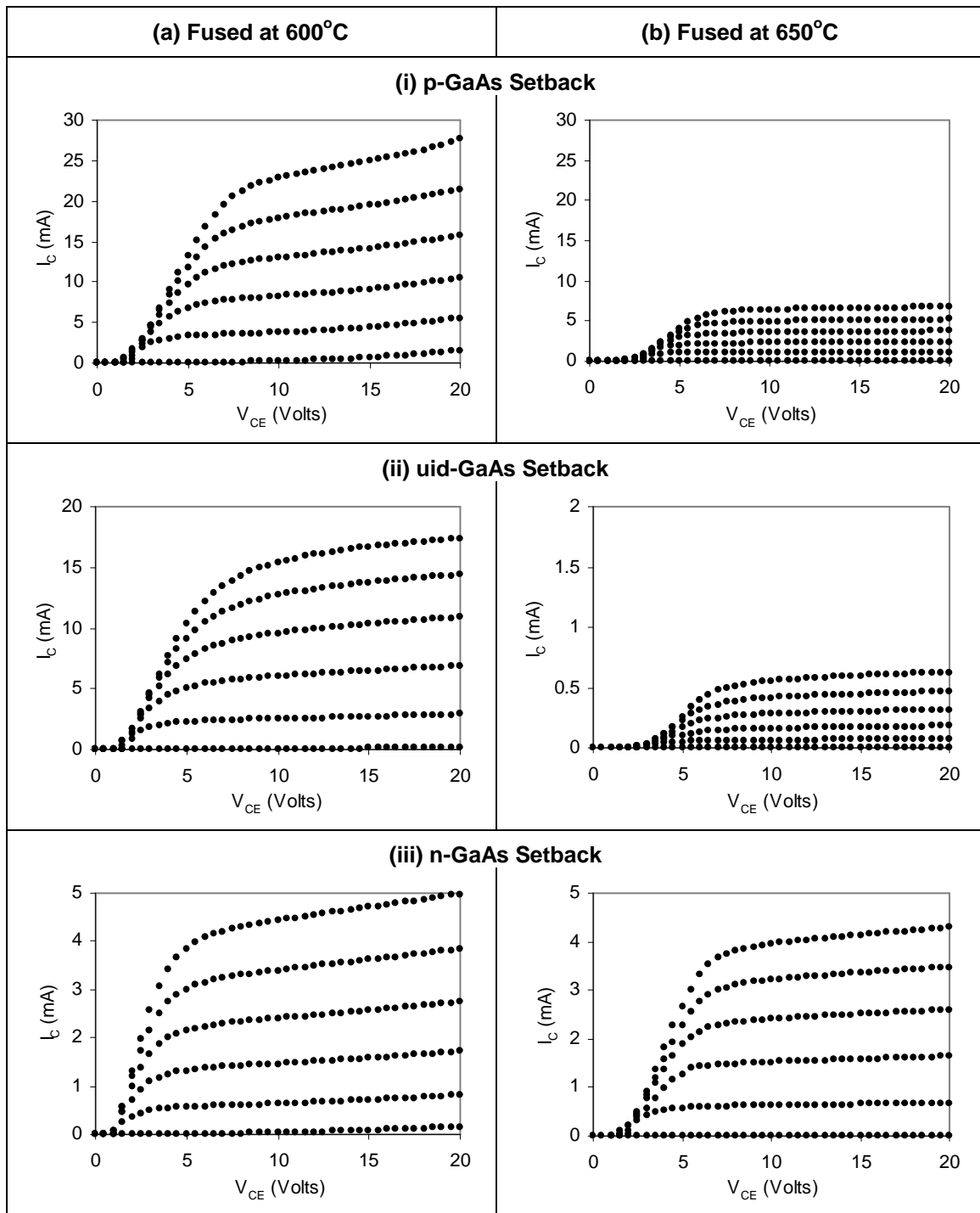


Figure 5.15. Common-emitter I-V characteristics of HBTs formed via wafer fusion for one hour at (a) 600°C and (b) 650°C. HBTs had a base-collector setback material of (i) p-GaAs lightly doped with carbon, (ii) uid-GaAs, and (iii) n-GaAs lightly doped with Si. Setback layers were 20nm thick. I_B step size was 2mA.

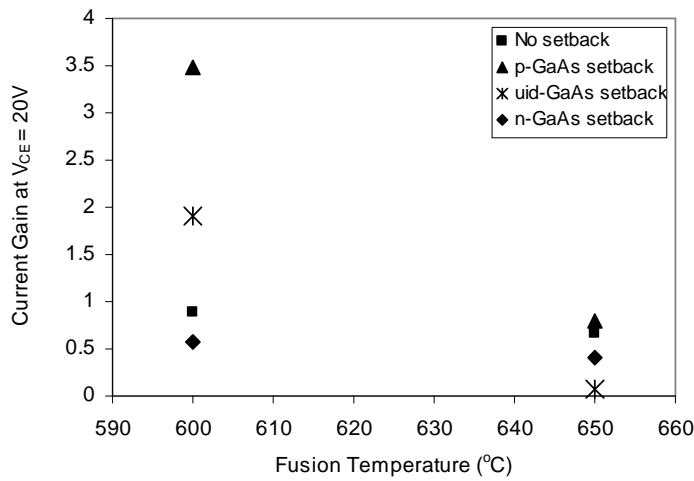


Figure 5.16.a. Common-emitter current gain (β), at $I_B=10\text{mA}$, of various HBT structures formed via wafer fusion at 600-650°C for one hour. The HBTs had either no base-collector setback layer or a setback material of uid-GaAs, p-GaAs lightly doped with carbon, or n-GaAs lightly doped with Si. Setback layers were 20nm thick.

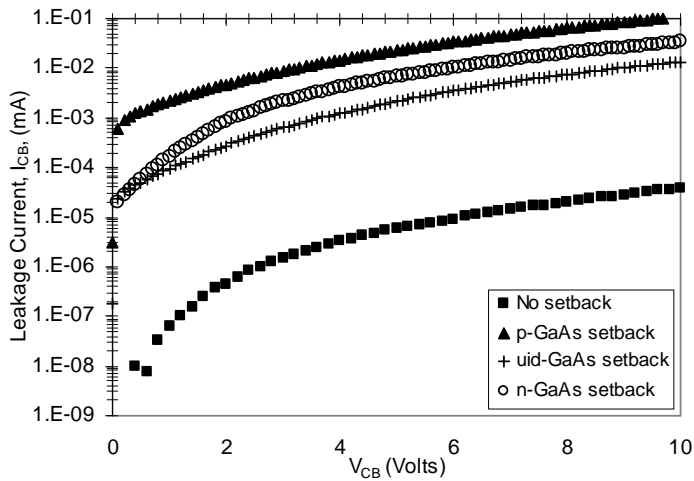


Figure 5.16.c. Base-collector leakage current (measured with the emitter open) in various HBT structures formed via wafer fusion at 600°C for one hour. The HBTs had either no base-collector setback layer or a setback material of uid-GaAs, p-GaAs lightly doped with carbon, or n-GaAs lightly doped with Si. Setback layers were 20nm thick.

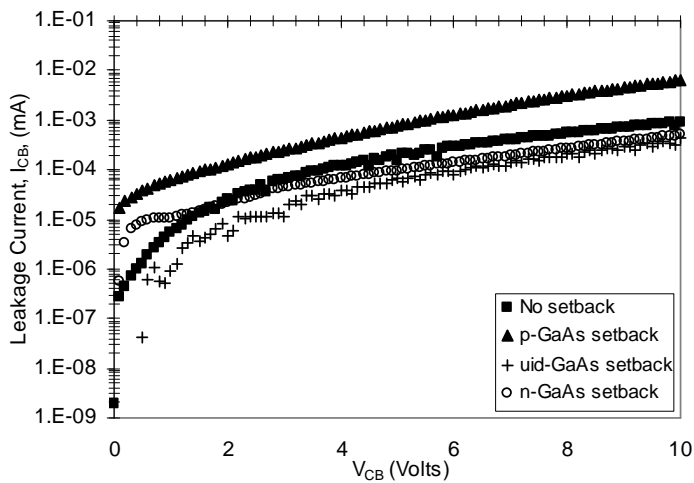


Figure 5.16.c. Base-collector leakage current (measured with the emitter open) in various HBT structures formed via wafer fusion at 650°C for one hour. The HBTs had either no base-collector setback layer or a setback material of uid-GaAs, p-GaAs lightly doped with carbon, or n-GaAs lightly doped with Si. Setback layers were 20nm thick.

5.6. References

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