Chapter 2. Fusion Process and Analytical Techniques

2.1. Overview

This chapter begins by describing the wafer fusion process. Despite the many challenges described in Chapter 1, a reliable, reproducible wafer fusion process was developed and demonstrated to form a number and variety of mechanically robust and electrically active GaAs-GaN heterojunctions. Table 2.1 lists the 45 samples designed, fabricated, and tested via electrical (I-V) measurements throughout the course of this project. The devices were AlGaAs-GaAs-GaN HBTs (with and without a base-collector setback layer), AlGaAs-GaAs-GaAs HBTs, p-GaAs/n-GaN diodes, and simple n-GaAs/n-GaN heterojunctions. This list does not include the numerous samples successfully formed via fusion, for chemical and structural studies.

As described in Chapter 1, the quality of the fused base-collector junction was studied via electrical, chemical, and structural techniques. Additionally, it was necessary to monitor diffusion effects on the *entire* device materials structure, as the entire device was subjected to high fusion temperatures (500-750^{o}C)for long times (0.25-2 hours). After fusion and GaAs substrate removal, device layers were accessible for one of the following analytical methods: electrical current-voltage (I-V) testing, secondary ion mass spectrometry (SIMS), or high-resolution transmission electron microscopy (HRTEM). Each analytical technique is briefly described in the remainder of this chapter. Information from the chemical (SIMS) and structural (TEM) analyses helped in assessing the reasons for variations observed in the electrical (I-V) performance of devices fused over a wide range of systematically varied temperatures and times.

2.2. Wafer Fusion Process and Development

2.2.1. Pre-fusion Surface Preparation

The basic process for pre-fusion surface preparation was established by D. Babic [1], N. Margalit [2], K.A. Black [3], and other former graduate students advised by Professors Evelyn Hu and John Bowers in the Materials and Electrical and Computer Engineering Departments at the University of California at Santa Barbara. The basic process, as designed for GaAs-InP fusion for vertical-cavity lasers, is detailed in Table 2.2. This process has not been well characterized and

optimized, and leaves much room for improvement, as discussed in detail in Chapter 7's suggestions for future work. Ideally, surface preparation would be done in an oxygen-free ambient, in order to minimize residual surface oxides that would ultimately contaminate the fused interface. Also, surface preparation would ideally be optimized by analysis (e.g. Auger) of the surface after each process step, in order to ensure minimization of surface oxides and contaminants such as photoresist residue. For example, in Table 2.2, the two oxidation steps are each followed immediately by oxide removal steps. However, no analysis has been done to ensure that the surface oxide, prior to these steps, is effectively reduced rather than increased by these steps. In fusing the HBTs of this dissertation study, the oxidation steps were omitted from the process.

The process step of etching "escape" channels was also omitted in fusing the HBTs of this dissertation study. Escape channels are generally used to prevent gas and liquid from being trapped at the fused interface, where they might otherwise prevent bonding of the two wafers. Without channels in GaAs-InP, Si-Si, and Si-SiO_2 fusion [3-6], a large density of bubbles (~100um) and smaller voids (~1um) were observed at the fused interface. With channels, such defects were successfully mitigated. At the start of this project, GaAs and GaN were fused with the use of escape channels. However, the SIMS data (Figure 2.1) suggested that the presence of the escape channels may have increased contamination of the fused interface. Figure 2.1 shows SIMS data for seven different samples, each fused at 500-750^{o}C for 1 hour. SIMS data consistently revealed strong carbon and oxygen signals at the fused

interface. C and O may have originated from residual surface impurities on the GaAs and GaN surfaces prior to fusion. However, an increase of these signals with elevated fusion temperature suggested that C and O may have also originated from deep in the bulk materials or from the escape channels. It is interesting to consider the double peak in the oxygen signal at the fused interface. The double peak is discussed in Section 2.4.

In order to assess if escape channels and oxidation processes (steps 2 and 5-7 of Table 2.2) were required for bubble-free fusion of GaAs-GaN, two samples of an identical HBT materials structure (Figure 2.2a) were fused under the same thermal conditions (750^{o}C for 1 hour). One sample (Figure 2.2.i) underwent the entire surface preparation process detailed in Table 2.2, whereas the other sample (Figure 2.2.ii) did not undergo steps 2 and 5-7. In both fused samples, no bubbles were observed at the fused interface. This suggested that escape channels and oxidation processes were not required in the pre-fusion surface preparation of mechanically robust AlGaAs-GaAs-GaN HBTs. However, the I-V data (Figure 2.2) revealed that electrical performance did improve with the additional surface preparation. Thus, because the escape channels and oxidation processes were not included in the pre-fusion surface preparation of the HBTs described in this dissertation, this work has much potential for further improvement, with improved pre-fusion surface preparation.

2.2.2. Fusion Process

This study begins by examining the quality of simple fused GaAs-GaN structures, and uses those data to determine the starting points of the process for the AlGaAs-GaAs-GaN fused HBT. Hence, three wafer-fused device structures were studied initially: (1) the n-GaAs/n-GaN heterojunction, henceforth called the "n-n structure", (2) the p-GaAs/n-GaN diode, called the "p-n structure", and (3) the n-AlGaAs/p-GaAs/n-GaN HBT.

The wafer fusion process is depicted in Figure 2.3. (Al)GaAs structures were grown by molecular beam epitaxy (MBE) at 585^{o}C in a Varian Gen-II system. MBE structures were grown by various graduate students at the University of California at Santa Barbara in the Electrical and Computer Engineering and Materials Departments: Andrew Huntington and Chad Wang advised by Larry Coldren, Lidong Zhang advised by Evelyn Hu, and Sheila Mathis advised by James Speck. GaN structures were grown by metal-organic chemical vapor deposition (MOCVD) on c-plane (0001) sapphire at 1160^{o}C. MOCVD structures were grown by various graduate students at the University of California at Santa Barbara in the Electrical and Computer Engineering and Materials Departments: Andreas Stonas advised by Evelyn Hu and Steven DenBaars, and Tal Margalith advised by Larry Coldren and Steven DenBaars.

(Al)GaAs and GaN were cleaved into rectangles (5-10mm x 5-10mm), solvent-cleaned in acetone and isopropanol, soaked in NH_4OH for oxide removal, rinsed in methanol, joined together in methanol, and annealed ("wafer-fused") under

a uniaxial pressure of 2 MPa in a nitrogen ambient. Structures were fused over a wide range of systematically varied temperatures (500-750^{o}C) and times (0.25-2 hours). After fusion, the GaAs substrate was removed via wet etching in H_2O_2:NH_4OH. This selective etch terminated at the AlAs layer, which was subsequently removed in HF. After the GaAs substrate removal, device layers were accessible for one of the analytical methods described in the remainder of this chapter.

2.3. Electrical Analysis via I-V

After wafer fusion and substrate removal, as described in Section 2.2, samples were sculpted into HBT or diode structures for I-V testing. For the HBT structure, n-AlGaAs emitter mesas ($1x10^{-5}cm^2$) and p-GaAs base mesas ($5x10^{-5}cm^2$) were defined via wet etching in H_3PO_4:H_2O_2:H_2O. For the diode structures, larger GaAs mesas ($100x100um^2$) were wet-etched. n-GaAs ohmic contacts (from bottom to top) were Ni/AuGe/Ni/Au annealed at 415^{o}C for 5 seconds, p-GaAs ohmic contacts were Zn/Au and n-GaN ohmic contacts were unannealed Al/Au. For the GaAs-GaN diode structures (Chapter 3), the p-GaAs contacts were annealed at 190^{o}C for 10 seconds. For the AlGaAs-GaAs-GaN HBTs (Chapters 4-5), the p-GaAs contacts were unannealed, in order to prevent the metals from spiking completely through the thin GaAs base (100-150nm) to the GaN collector. For the AlGaAs-GaAs-GaAs HBTs (Chapter 6), the emitter contacts were first annealed alone at

415^{o}C for 5 seconds, and then all contacts were annealed together at 415^{o}C for 5 seconds.

Several I-V samples of an identical material structure were fused over a wide range of systematically varied temperatures (500-750^{o}C) and times (0.25-2 hours). The I-V data for each sample were then compared with the others, as shown for example in Figures 3.3 and 3.4. Variations in device electrical performance were observed and correlated with the systematically varied fusion conditions.

In order to assess and improve device electrical performance, energy band diagrams were needed. The construction of an accurate band diagram was challenging, as the conduction band offset (ΔE_C) of the wafer-fused GaAs-GaN base-collector junction was unknown. During wafer fusion of the base-collector junction, uncontrolled bond reconstruction or residual impurities may have produced electronic traps or barriers leading to a positive ΔE_C in the energy band diagram. Additionally the natural material properties of the GaAs-GaN heterojunction (regardless of any fusion-induced conduction band traps or barriers) may have led to an inherently positive ΔE_C.

In 1998, the first GaAs-GaN heterojunction was formed via wafer fusion by Lee McCarthy (at that time, a graduate student in the Electrical and Computer Engineering Department at the University of California at Santa Barbara).[7] McCarthy *et al.* made a first-order attempt to determine the ΔE_C of the wafer-fused junction by assuming a thermionic barrier and analyzing the diode characteristics measured over a wide range of temperatures. (McCarthy's analysis was designed

according to earlier work done by T.H. Lim *et al.* on epitaxially grown $Ga_{0.52}In_{0.48}P$/GaAs junctions.[8]) Following McCarthy's example, a similar analysis was done on the wafer-fused GaAs-GaN base-collector junction of an HBT fused at 600°C for 1 hour. Figure 2.4.a shows the base-collector diode characteristics (taken with the emitter open) of the same HBT device measured at 300-400K. A thermionic barrier (ϕ) of 0.4eV was extracted by fitting these data (Figure 2.4.b) to the relationship:

$$I_{BC} \sim I_0^* \cdot \exp\left[\frac{q(V_{BC} - \phi)}{k_B T}\right]$$

The estimated thermionic barrier was similar to that obtained by McCarthy *et al.* for their wafer-fused p-GaAs/n-GaN diode ($\phi \sim$ 0.6eV).[7] Much additional work (including capacitance-voltage measurements) would have been needed, in order to determine an accurate ΔE_C for the wafer-fused heterojunction. Additionally, it would have been interesting to assess if and how ΔE_C varied with the many fusion conditions and the many base-collector material designs studied throughout the course of this dissertation work. However, this first-order approximation was sufficient for simulating energy band diagrams, in order to design and evaluate device improvements. After simulating the energy band diagrams of various HBT materials structures, we then fabricated and tested the proposed device structures that seemed to correspond to the most favorable band diagrams.

2.4. Chemical Analysis via SIMS

Secondary ion mass spectrometry (SIMS) is a common beam technique for obtaining depth profiles of specific elements, isotopes, and molecular species. It is often used for dopant profiling in semiconductor characterization.[9] During SIMS testing, a primary ion beam impinges on the sample, ejecting secondary ions and neutral atoms. The mass-to-charge ratio of an ejected ion is detected as a mass spectrum or as a count of specific mass-to-charge ratios. For depth profiling, selected masses are plotted as secondary ion yield versus sputtering time. By using calibrated standards, with composition and matrices identical or similar to the unknown, one can convert ion yield to concentration, and sputtering time to depth.

Figures 2.5 and 2.6 show typical SIMS data from this dissertation study. Figure 2.5 shows the entire depth profile for a single HBT sample (with a 50nm base-collector setback layer lightly doped with C) formed via fusion at 600^{o}C for one hour. Figure 2.6 shows the same profile, but only at a depth near the fused GaAs-GaN interface. For each SIMS sample, depth profiles were obtained for dopants, impurities, and matrix species (Si, Be, C, H, O, GaN, GaAs). SIMS data were used extensively to monitor diffusion effects, which were aggravated with more elevated fusion temperatures and times. As with I-V samples, several SIMS samples of an identical material structure were fused over a wide range of systematically varied temperatures (500-750^{o}C) and times (0.25-2 hours). The SIMS data for each sample were then compared with the others, as shown for example in Figures 4.3 and 6.2. It

was important to monitor the chemical composition of the various samples, in order to assess the reasons for variations observed in device electrical performance.

Interpretation of SIMS data can be difficult. For this dissertation study, two key issues were troublesome: the matrix effect and cascade mixing.[9] The matrix effect refers to strong variations in secondary ion yield for a single element in various matrices. For example, Figure 2.6 seems to indicate that the Si concentration was higher in the GaN (~10^{17} Si atoms per cm^3) than in the GaAs (~10^{15} Si atoms per cm^3). However, although this may be true, SIMS data should not be used as evidence for such a statement. Due to the matrix effect, the Si signal in the GaN (~100 counts per second) may have been stronger than the Si signal in the GaAs (~2 counts per second), even if the actual Si concentration in the GaN was the same or lower than in the GaAs. (It is important to realize, in Figure 2.6, the right vertical axis is ion counts per second, which represents the actual data. The left vertical axis is concentration, which was obtained by simply comparing the counts per second to a calibration for the GaAs matrix only.) For this reason, in this dissertation study, SIMS is used only to compare ion yields in the same matrix. For example, from Figure 3.9.a, it would be inappropriate to conclude that the Si concentration in the GaAs was lower than in the GaN. However, assuming that the matrix at the fused interface was similar for all samples, it would be accurate to state that the Si concentration at the fused interface was higher for the samples fused for reduced times (0.25-0.5 hour), and the Si concentration at the fused interface was lower for the sample fused for a longer time (1 hour).

It is interesting that the matrix effect may explain the double peak at the fused interface, sometimes observed for the oxygen and carbon signals (as shown, for example, in Figure 2.6). It would be inappropriate to conclude that oxygen and carbon are depleted at the fused interface, yet aggregated near the fused interface. Although this may indeed be true, it is more likely that the vicinity of the fused interface consists of a non-uniform matrix (especially considering the disordered interface shown via TEM in Figure 2.7 and discussed in Section 2.5), and the ion yields for carbon and oxygen fluctuated with the variation in the matrix.

Cascade mixing is the second effect that can complicate SIMS analysis. During SIMS testing, as primary ions strike sample atoms and displace them from their lattice positions, these newly sputtered atoms are added to a mix of recently sputtered atoms. As ions in the mix are eventually ejected and detected, the data will indicate a longer depth profile than the actual depth profile of the sample. For example, Figure 2.6 seemed to suggest that all species first accumulated at the fused interface, and then diffused away from the fused interface into the surrounding materials, diffusing more extensively into the GaN than into the GaAs. However, due to cascade mixing (and to the decreased likelihood of diffusion in GaN, as compared to GaAs), it is much more likely that the distribution in the GaN is shown to be higher than the actual distribution. This limitation is unfortunate, as copious SIMS data were taken of samples fused over a wide range of annealing conditions (500-750^{o}C, 0.25-2 hours). Those data might have been used to estimate diffusion constants of the various dopants and impurities (Si, Be, C, O) in GaAs and GaN. A

suggestion for future work is to obtain SIMS profiles from both directions (from GaAs to GaN, and also from GaN to GaAs). By overlapping the two sets of data, accurate depth profiles are much more likely.

SIMS data were obtained in collaboration with one of three service providers: Yumin Gao at Applied Microanalysis Labs, Inc., Patrick van Lierde at Charles Evans & Associates, or Tom Mates at the University of California at Santa Barbara.

2.5. Structural Analysis via TEM

Wafer-fused interfaces can be disordered over several monolayers, with amorphous interlayers (often identified as oxides) forming between the two constituent wafers. By cross-sectional high resolution transmission electron microscopy (HRTEM), it was determined that the GaAs-GaN interface described in this dissertation (formed via fusion at 550-750^{o}C for 0.25-1 hour) exhibited disorder which is limited to 0.5-2nm (Figure 2.7). This compared favorably to other fused semiconductor materials. Shi *et al.* observed an interlayer thickness of 5nm at GaAs-GaAs interfaces fused at 400^{o}C for 1hour.[10] Black and Jin-Phillipp *et al.* observed an interlayer thickness of 6-8nm at GaAs-InP junctions fused at 630^{o}C for <0.5 hour.[6, 11] At the GaAs-GaN interface, the disorder may have been more limited due to the higher bond strength of GaN, as compared to GaAs or InP.

In Figure 2.7, the disordered interlayer of bright contrast was most likely amorphous material. Moreover, the interlayer may have been an oxide, given the

presence of oxygen confirmed by both SIMS and energy dispersive x-ray (EDX) analyses (Figures 2.6 and 2.8). The interlayer thickness varied with fusion temperature, from 0.5-1nm in samples fused at 750^{o}C, to 1.5-2nm in a sample fused at 550^{o}C. The elevated disorder (whether oxide or not), present in samples fused at lower temperatures, may have contributed to variations in electrical characteristics observed for samples fused over a wide range of temperatures (500-750^{o}C).

Plan-view TEM suggested that Ga-As and Ga-N bond rearrangement may not have happened during fusion, as there was no indication of a dislocation network accommodating the GaAs-GaN lattice mismatch. When different materials are fused together, their lattice mismatch is accommodated by a network of misfit dislocations with an edge component in the plane of fusion. If the orientations of the adjoining crystals are relatively twisted in-plane, dislocations with a screw component are also formed in order to accommodate the twist. Therefore, a two-dimensional network (a regular grid of misfit dislocations with Burger's vectors in the plane of fusion) should appear at the interface, when two twisted, lattice-mismatched crystals are wafer-fused. Such a grid was observed for bonded cubic crystals.[12-14] However, in this dissertation study, no closely-spaced, regular grid of dislocations was observed. Similarly, this type of dislocation network was not observed with a wafer-fused sapphire-GaAs interface.[15, 16] The reason is likely to involve the thermal inertness of the constituent materials. The high melting point of GaN (T_m>1200^{o}C [17]) or sapphire (T_m>2000^{o}C), relative to fusion temperatures (500-750^{o}C) may

have precluded actual chemical bonding between the GaN (or sapphire) and GaAs. To understand this further, more detailed studies would be necessary.

The GaAs-GaN fused interface of this dissertation study was examined via TEM and EDX in collaboration with Jacek Jasinski and Zuzanna Liliental-Weber at the Lawrence Berkeley National Laboratory. Detailed analyses of EDX, and of cross-sectional and plan-view TEM, were published elsewhere.[18, 19]

Simple n-GaAs/n-GaN Heterojunctions: Figure 3.1.a		
Sample ID	Fusion Temperature (^{o}C)	Fusion Time (hours)
N39	750	0.5
N42	650	1
N46	700	1
N44	750	1
N38	650	2
N41	700	2
N35	750	2
p-GaAs (Be-doped)/n-GaN Diodes: Figure 3.1.b		
Sample ID	Fusion Temperature (^{o}C)	Fusion Time (hours)
N51	750	0.5
N43	650	1
N47	700	1
N45	750	1
N58	650	2
N57	700	2
N53	750	2
p-GaAs (C-doped)/n-GaN Diodes: Figure 3.1.b		
Sample ID	Fusion Temperature (^{o}C)	Fusion Time (hours)
N87	550	0.25
N85	550	0.5
N83	500	1
N89	525	1
N81	550	1
N79	600	1
N77	650	1
N75	700	1
N73	750	1
Simple AlGaAs-GaAs-GaN HBT: Figure 4.1		
Sample ID	Fusion Temperature (^{o}C)	Fusion Time (hours)
H15	550	1
H13	600	1
H14	650	1
H12	700	1
H11	750	1

AlGaAs-GaAs-GaN HBT with setback layer: Figure 5.1.ii or 5.1.iii				
Sample ID	Fusion Temp. (^{o}C)	Fusion Time (hours)	Setback Dopant	Setback Width (nm)
Sba10	600	1	Si (high concentration)	20
Sbb12	600	1	Si (high concentration)	50
Sba8	650	1	Si (high concentration)	20
Sbb10	650	1	Si (high concentration)	50
Sba6	750	1	Si (high concentration)	20
Sbb8	750	1	Si (high concentration)	50
Sa3	600	1	Si (low concentration)	20
Sa1	650	1	Si (low concentration)	20
Ca2	600	1	C	20
Ca1	650	1	C	20
Ua2	600	1	unintentionally doped	20
Ua1	650	1	unintentionally doped	20

AlGaAs-GaAs-GaAs HBT: Figure 6.1.b			
Sample ID	Fusion/Anneal Temperature (^{o}C)	Fusion Time (hours)	Thermal Treatment
Aa1	n/a	n/a	as-grown, unannealed
Aa5	600	1	annnealed
Aa3	750	1	annealed
Ab3	600	1	fused
Ab1	750	1	fused

Table 2.1. Samples designed, fabricated, and tested via electrical (I-V) measurements throughout the course of this dissertation project.

Step	Description
1	Cleave wafers into rectangles of 5-10mm x 5-10mm.
2	Etch escape channels into the GaAs sample. Channels are 150-250nm deep and 10um wide, and extend over the entire surface in a cross-hatch pattern of 150um x 400um.
3	Solvent-clean in acetone, then isopropanol. Blow dry with nitrogen.
4	Scrub with a cotton swab under an acetone spray.
5	Oxidize for 10 minutes in a plasma etcher. This step is especially important for photoresist descum after the photolithography associated with the etching of escape channels (in Step 2).
6	Remove the oxide with a 2-minute soak in NH_4OH.
7	Oxidize for 1 hour in UV/ozone oven.
8	Remove the oxide with a 10-minute soak in NH_4OH.
9	Transfer to a passivation medium (methanol, NH_4OH, or HF).

Table 2.2. The basic process for pre-fusion surface preparation was developed by D. Babic [1], N. Margalit [2], K.A. Black [3], and other former graduate students advised by Professors Evelyn Hu and John Bowers at the University of California at Santa Barbara.

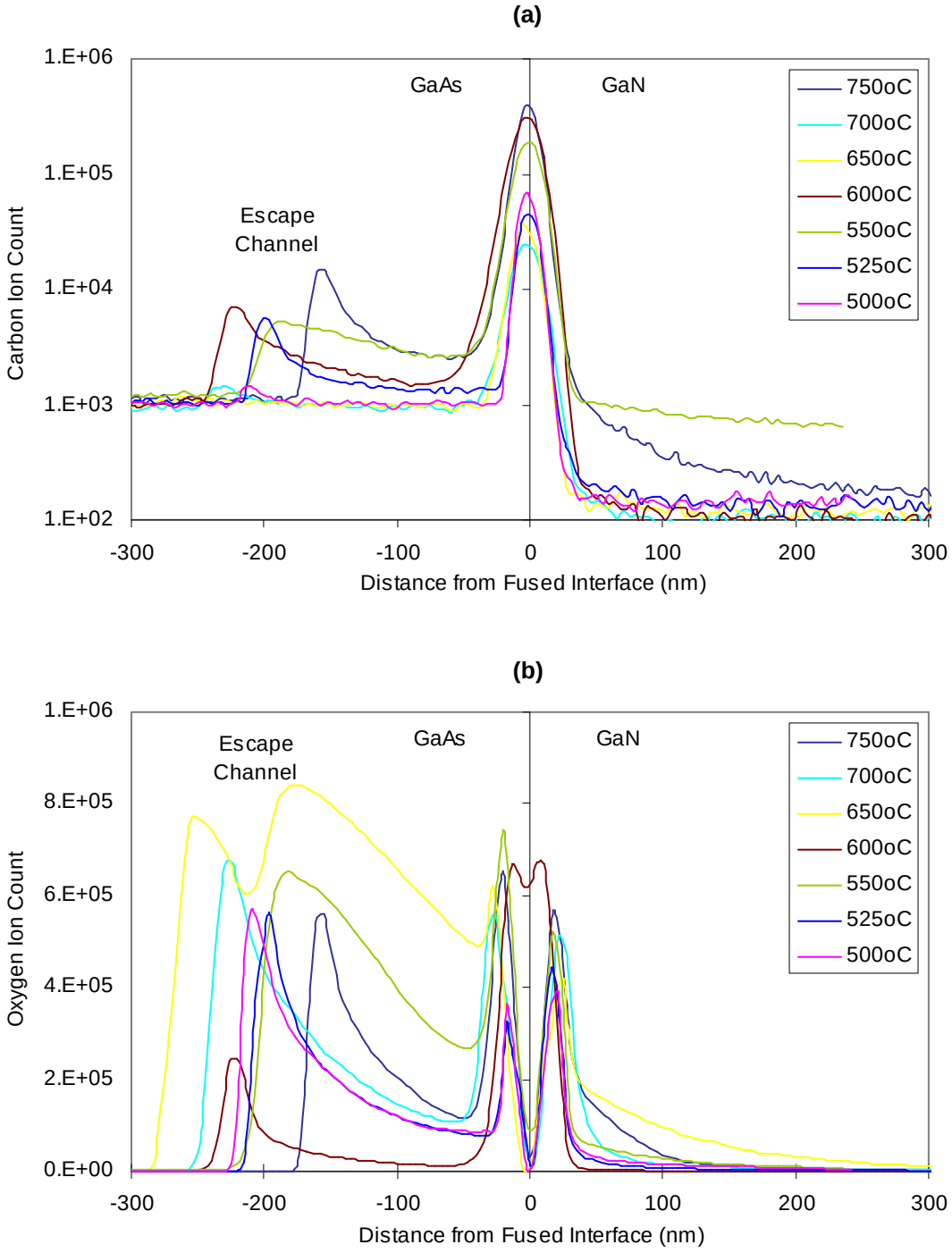


Figure 2.1. Depth profiles of (a) carbon and (b) oxygen near the wafer-fused GaAs-GaN interface, as obtained via secondary ion mass spectroscopy (SIMS). Data are shown for seven different samples of an identical material structure, each fused at 500-750^{o}C for 1 hour. These SIMS data were obtained in collaboration with Tom Mates at the University of California at Santa Barbara.

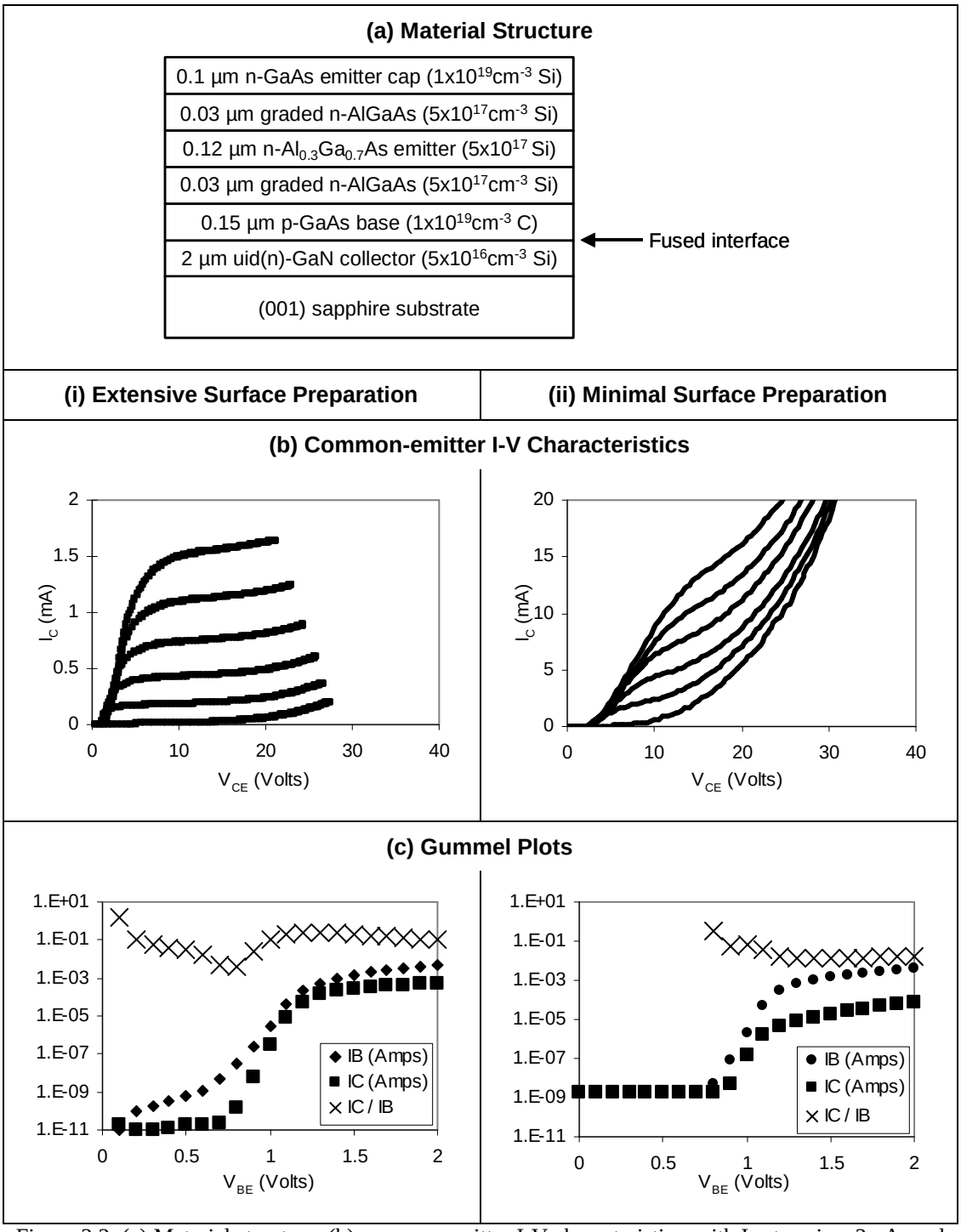


Figure 2.2. (a) Material structure, (b) common-emitter I-V characteristics, with I_B step size=2mA, and (c) Gummel plots for HBTs formed via fusion at 750°C for one hour. HBT (i) underwent the entire surface preparation process detailed in Table 2.1, whereas HBT (ii) did not undergo steps 2 and 5-7.

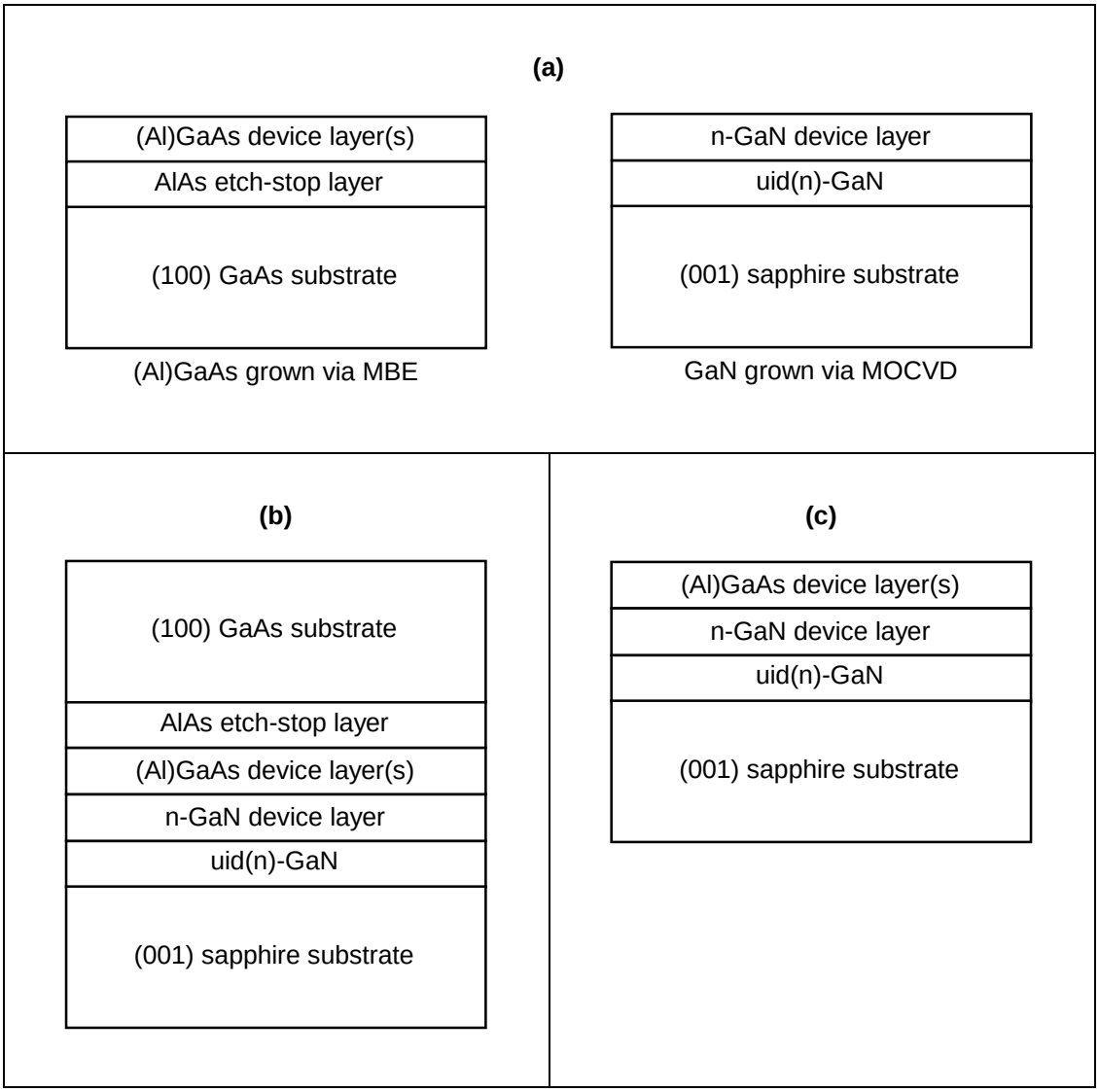


Figure 2.3. The wafer fusion process: (a) starting materials, (b) wafers during fusion, and (c) sample after fusion and GaAs substrate removal. After the fusion process, device layers are accessible for one of the following analytical methods: electrical current-voltage (I-V) testing, secondary ion mass spectroscopy (SIMS), or high-resolution transmission electron microscopy (HRTEM).

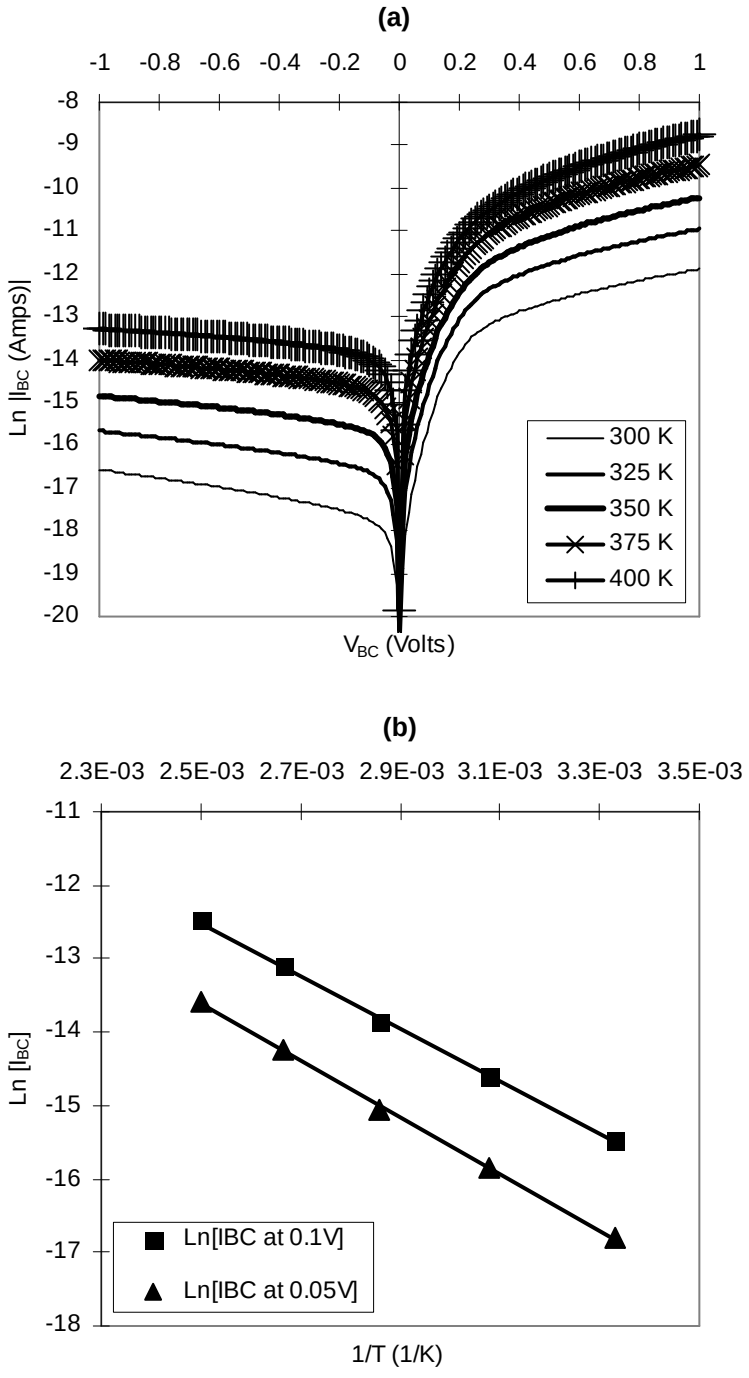


Figure 2.4. (a) Base-collector diode I-V characteristics (taken with the emitter open) of a single HBT device measured at 300-400K, and (b) the same data graphed for extraction of the thermionic barrier.

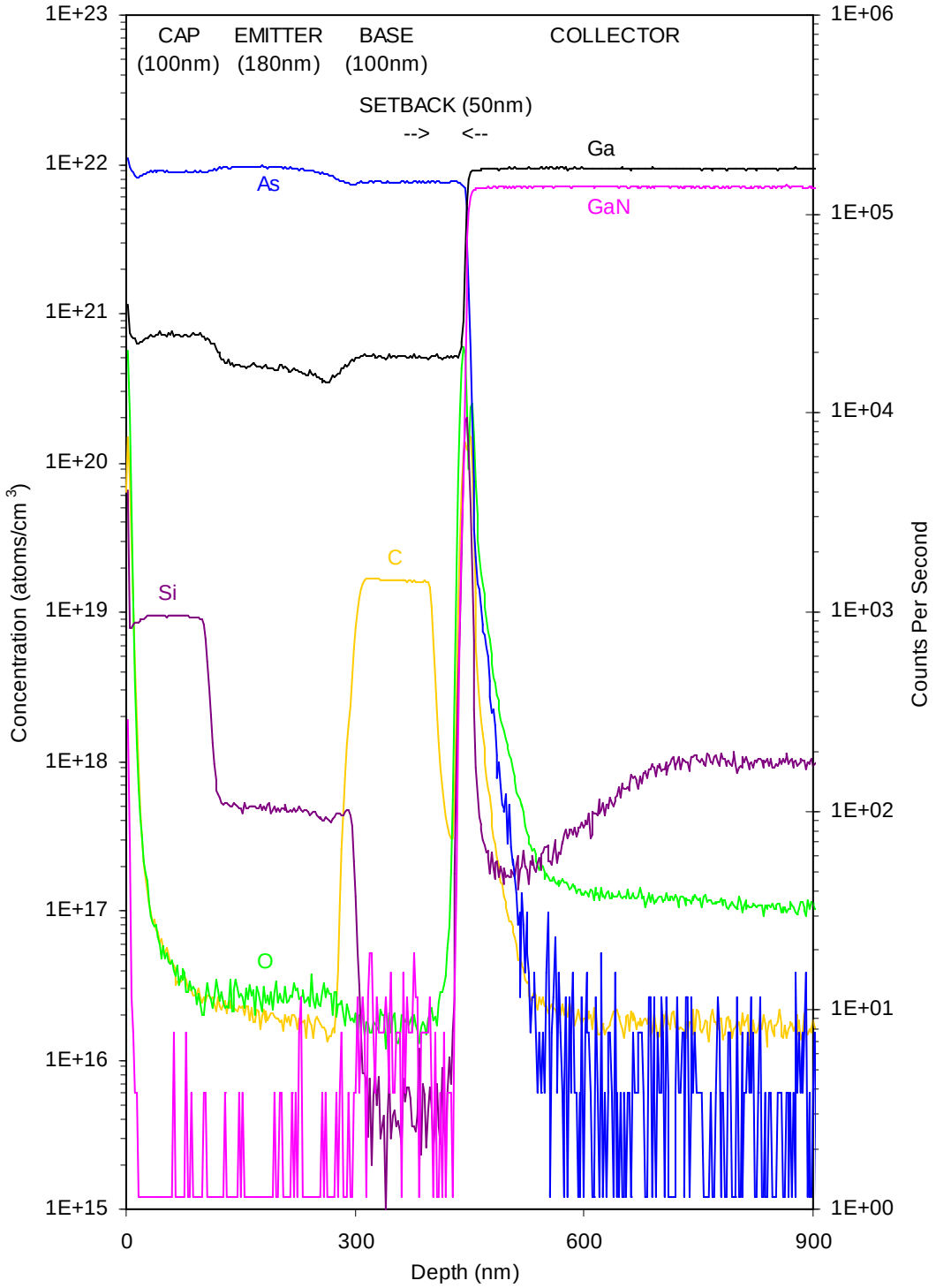


Figure 2.5. Depth profile obtained via secondary ion mass spectrometry (SIMS). This HBT sample was formed via wafer fusion at 600°C for one hour. These SIMS data were obtained in collaboration with Charles Evans & Associates.

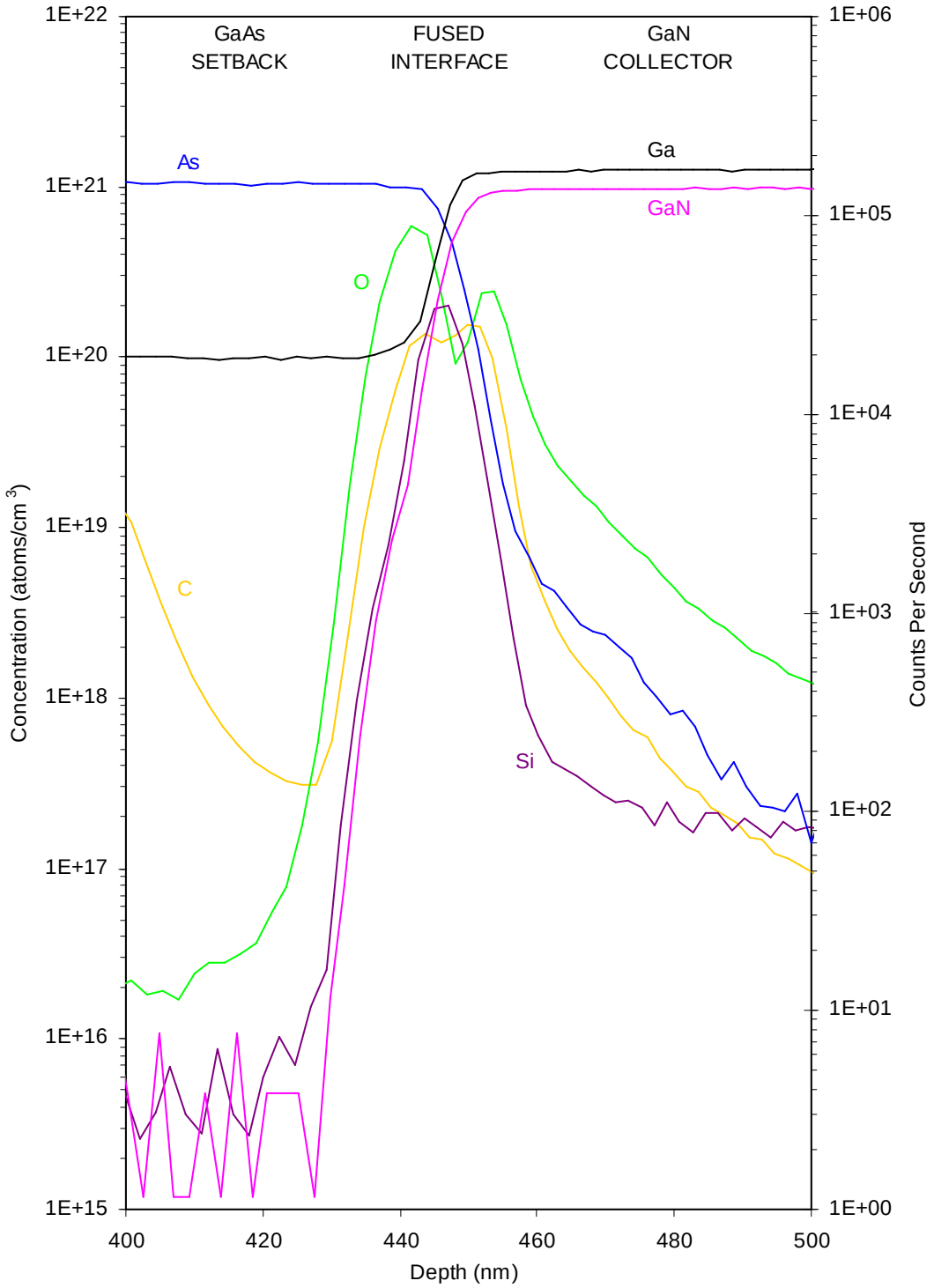


Figure 2.6.Depth profile near the fused interface, obtained via secondary ion mass spectrometry (SIMS). This HBT sample was formed via wafer fusion at 600^{o}C for one hour. These SIMS data were obtained in collaboration with Charles Evans & Associates.

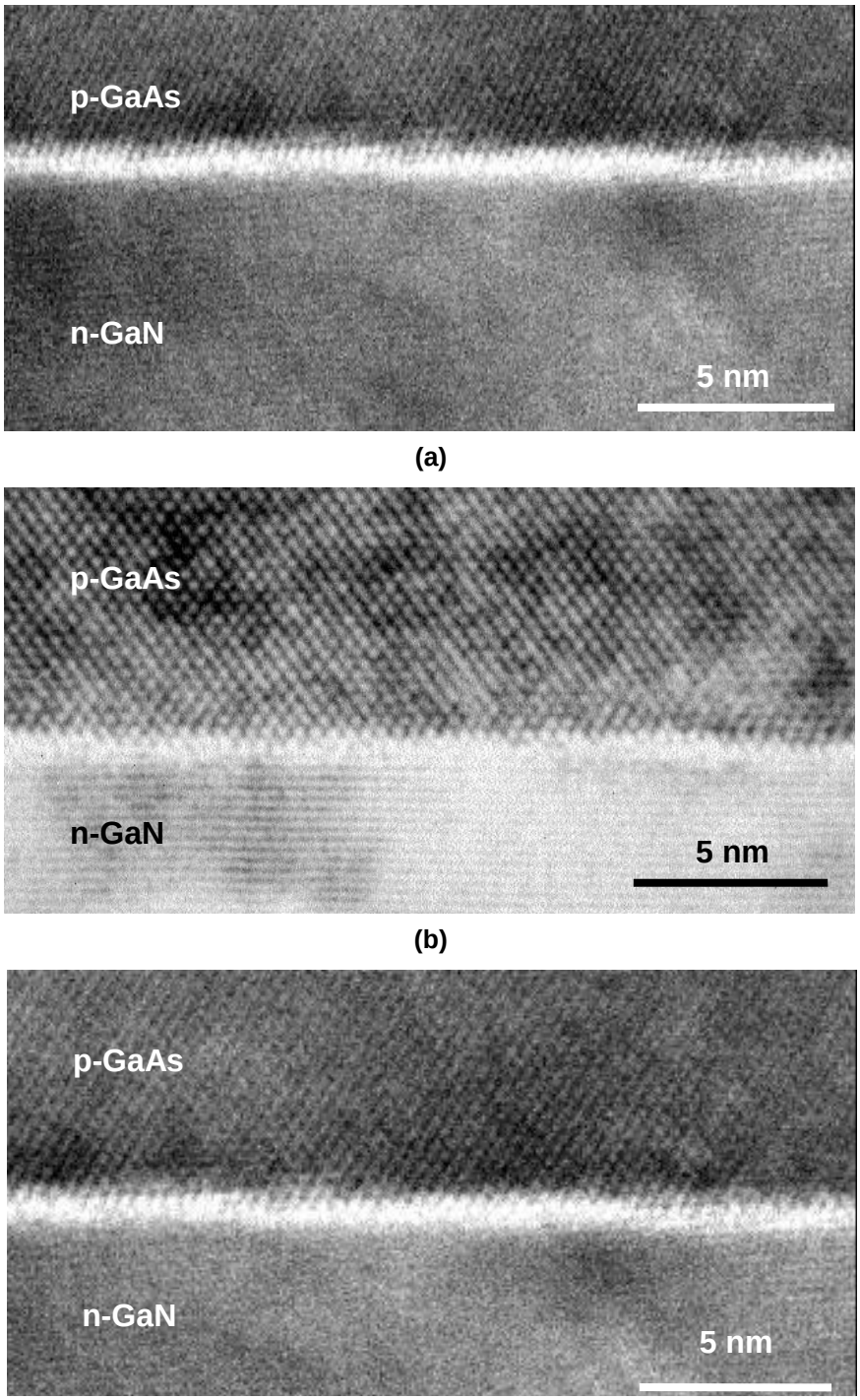
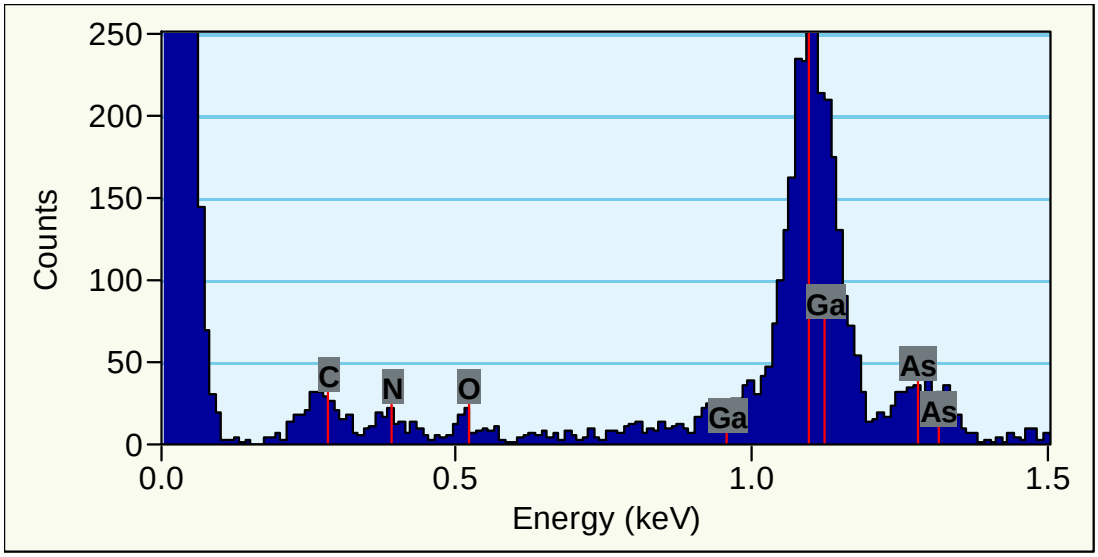
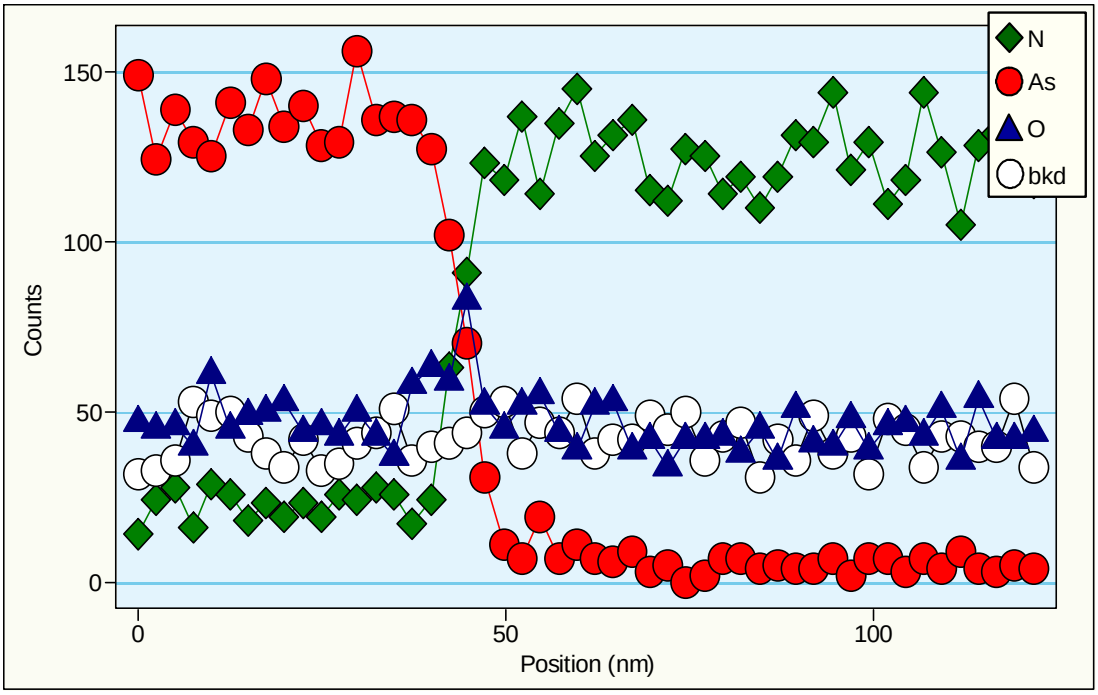


Figure 2.7. HRTEM of the GaAs-GaN interface wafer-fused under various conditions: (a) at 750^{o}C for 0.25hr, (b) at 750^{o}C for 1hr, and (c) at 550^{o}C for 1hr. These images were obtained in collaboration with J. Jasinski and Z. Liliental-Weber at the Lawrence Berkeley National Laboratory.



(a)



(b)

Figure 2.8. Oxygen at the wafer-fused GaAs-GaN interface, as shown by energy dispersive x-ray, EDX. The interface was fused at 750^{o}C for one hour. EDX data were obtained in collaboration with J. Jasinski and Z. Liliental-Weber at LBNL.

2.6. References

[1] D. I. Babic, K. Streuble, R. P. Mirin, N. M. Margalit, J. E. Bowers, E. L. Hu, D. E. Mars, L. Yang, and K. Carey, "Room-Temperature Continuous-Wave Operation of 1.54-Mu-Um Vertical-Cavity Lasers," *Ieee Photonics Technology Letters*, vol. 7, pp. 1225-1227, 1995.

[2] N. M. Margalit, K. A. Black, Y. J. Chiu, E. R. Hegblom, K. Streubel, P. Abraham, M. Anzlowar, J. E. Bowers, and E. L. Hu, "Top-emitting double-fused 1.5 mu m vertical cavity lasers," *Electronics Letters*, vol. 34, pp. 285-287, 1998.

[3] A. Black, A. R. Hawkins, N. M. Margalit, D. I. Babic, A. L. Holmes, Y. L. Chang, P. Abraham, J. E. Bowers, and E. L. Hu, "Wafer fusion: Materials issues and device results," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 3, pp. 943-951, 1997.

[4] H. Yamaguchi, S. Fujino, T. Hattori, and Y. Hamakawa, "Superjunction by Wafer Direct Bonding," *Japanese Journal of Applied Physics Part 2-Letters*, vol. 34, pp. L199-L202, 1995.

[5] S. J. Yun, K. Y. Ahn, K. S. Yi, and S. W. Kang, "Studies on Microvoids at the Interface of Direct Bonded Silicon-Wafers," *Journal of the Electrochemical Society*, vol. 139, pp. 2326-2330, 1992.

[6] K. A. Black, Ph.D. Dissertation: *Fused long-wavelength vertical-cavity lasers*, Materials Department, University of California, Santa Barbara, 2000.

[7] L. S. McCarthy, J. G. Champlain, P. Kozodoy, G. Parish, R. K. Sink, and U. K. Mishra, "First Demonstration of a GaAs/GaN Fused p-n Heterojunction," presented at TMS Electronic Materials Conference (Charlottesville, Virginia), 1998.

[8] T. H. Lim, T. J. Miller, F. Williamson, and M. I. Nathan, "Characterization of interface charge at $Ga_{0.52}In_{0.48}P$/GaAs junctions using current-voltage and capacitance-voltage measurements," *Applied Physics Letters*, vol. 69, pp. 1599-1601, 1996.

[9] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed., Wiley (New York, New York), 1998.

[10] F. Shi, K. L. Chang, J. Epple, C. F. Xu, K. Y. Cheng, and K. C. Hsieh, "Characterization of GaAs-based n-n and p-n interface junctions prepared

by direct wafer bonding," *Journal of Applied Physics*, vol. 92, pp. 7544-7549, 2002.

[11] N. Y. Jin-Phillipp, W. Sigle, A. Black, D. Babic, J. E. Bowers, E. L. Hu, and M. Ruhle, "Interface of directly bonded GaAs and InP," *Journal of Applied Physics*, vol. 89, pp. 1017-1024, 2001.

[12] M. Benamara, A. Rocher, P. Sopena, A. Claverie, A. Laporte, G. Sarrabayrouse, L. Lescouzeres, and A. PeyreLavigne, "Structural and electrical investigations of silicon wafer bonding interfaces," *Materials Science and Engineering B-Solid State Materials for Advanced Technology*, vol. 42, pp. 164-167, 1996.

[13] G. Patriarche, F. Jeannes, J. L. Oudar, and F. Glas, "Structure of the GaAs/InP interface obtained by direct wafer bonding optimised for surface emitting optical devices," *Journal of Applied Physics*, vol. 82, pp. 4892-4903, 1997.

[14] L. Sagalowicz, A. Rudra, E. Kapon, M. Hammar, F. Salomonsson, A. Black, P. H. Jouneau, and T. Wipijewski, "Defects, structure, and chemistry of InP-GaAs interfaces obtained by wafer bonding," *Journal of Applied Physics*, vol. 87, pp. 4135-4146, 2000.

[15] P. Kopperschmidt, G. Kastner, S. Senz, D. Hesse, and U. Gosele, "Wafer bonding of gallium arsenide on sapphire," *Applied Physics a-Materials Science & Processing*, vol. 64, pp. 533-537, 1997.

[16] S. Senz, P. Kopperschmidt, G. Kastner, and D. Hesse, "Phase identification of micro and macro bubbles at the interface of directly bonded GaAs on sapphire," *Journal of Materials Science*, vol. 33, pp. 2073-2077, 1998.

[17] W. Utsumi, H. Saitoh, H. Kaneko, T. Watanuki, K. Aoki, and O. Shimomura, "Congruent melting of gallium nitride at 6 GPa and its application to single-crystal growth," *Nature Materials*, vol. 2, pp. 735-738, 2003.

[18] J. Jasinski, Z. Liliental-Weber, S. Estrada, and E. Hu, "Transmission Electron Microscopy Studies of Electrical Active GaAs/GaN Interface Obtained by Wafer Bonding," presented at Materials Research Society (MRS) Spring Meeting (San Francisco, California), vol. 722, pp. K7.15.1-K7.15.6, 2002.

[19] J. Jasinski, Z. Liliental-Weber, S. Estrada, and E. Hu, "Microstructure of GaAs/GaN interfaces produced by direct wafer fusion," *Applied Physics Letters*, vol. 81, pp. 3152-3154, 2002.