Wafer-fused AlGaAs/GaAs/GaN heterojunction bipolar transistor

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We describe an *n*-AlGaAs/*p*-GaAs/*n*-GaN heterojunction bipolar transistor, formed via wafer fusion of a *p*-GaAs base to an *n*-GaN collector. Wafer fusion was carried out at 750 °C for 1 h. Devices utilized a thick base (0.15 μm) and exhibited limited common-emitter current gain (0.2–0.5) at an output current density of ~100 A/cm^2. Devices were operated to V_{CE} greater than 20 V, with a low V_{CE} offset (1 V). Improvements in both device structure and wafer fusion conditions should provide further improvements in device performance. © *2003 American Institute of Physics.*
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The large breakdown field and high anticipated saturation velocity of GaN make this novel material particularly promising for high-frequency, high-power devices. With this goal in mind, quite a few researchers are working to develop GaN-based heterojunction bipolar transistors (HBTs).[1–5] Although results have been promising, there remain a number of outstanding materials issues. For example, AlGaN–GaN HBTs appear to be limited by large acceptor ionization energies and low hole mobilities.[6] A HBT structure utilizing AlGaAs–GaAs for the emitter base, with GaN as the collector, could potentially combine the high-breakdown voltage of GaN with the high mobility of the technologically mature AlGaAs–GaAs heterostructure. Because the high degree of lattice mismatch between GaAs and GaN precludes an all-epitaxial formation of this device, we have formed the GaAs–GaN heterostructure via a technique called wafer fusion. This letter reports the dc device characteristics of a wafer-fused HBT, and demonstrates the potential of wafer fusion for electrically active heterojunctions between lattice-mismatched materials.

The AlGaAs–GaAs emitter base was grown by molecular beam epitaxy (MBE) at 585 °C in a Varian Gen-II system. A sacrificial layer of undoped AlAs (0.5 μm) was grown on a (100) Si-doped n^+GaAs substrate, followed by growth of a contact layer (0.1 μm n^+GaAs, 1×10^{19} Si), the emitter (0.12 μm nAl$_x$Ga$_{1-x}$As flanked on top and bottom by 0.03 μm Al graded from $x=0$ to 0.3, all doped with 5×10^{17} Si), and finally the base layer (0.15 μm p^+GaAs, 1×10^{19} C). Carbon, rather than beryllium, was chosen as the *p*-type dopant in order to minimize dopant diffusion during the subsequent high-temperature fusion procedure. The *n*-GaN collector ($\sim5\times10^{16}$ Si) was grown by metalorganic chemical vapor deposition on *c*-plane (0001) sapphire at 1160 °C.

"Escape channels" were etched into the GaAs surface, to prevent liquid and gas from being trapped at the interface during subsequent fusion of GaAs and GaN. The wafers were cleaved into rectangles (5–10 mm) and cleaned with acetone and isopropanol. In order to minimize surface contamination, the wafers underwent two alternating oxidation and oxide removal steps. GaN and GaAs were rinsed and joined together in methanol, and annealed at 750 °C for 1 h in N_2 under 2 MPa of uniaxial pressure. After fusion, the GaAs substrate and AlAs etch stop were removed sequentially via selective wet etching. Onto the *n*-GaAs emitter cap layer, AuGeNi contacts were deposited and annealed at 415 °C. Emitter (1×10^{-5} cm^2) and base mesas (5×10^{-5} cm^2) were defined via wet etching. Unannealed ZnAu and AlAu contacts were made to the *p*-GaAs base and *n*-GaN collector, respectively.

Since the characteristics of the *n-p-n* HBT must depend on the behavior of the two constituent back-to-back diodes, we first examine the current–voltage ($I-V$) characteristics of the base-collector and emitter-base junctions. Figure 1 is the $I-V$ of the fused GaAs–GaN base-collector junction. The fused interface exhibits an ideality factor (n) of 2.5. It may appear that the wafer fusion produces a high value of n; we note that epitaxially grown GaN *p-n* junctions have also been reported with high ideality factors ($n\sim1.5$–9).[7,8] The AlGaAs–GaAs emitter-base junction is formed directly through MBE growth, but the 750 °C fusion temperature may degrade the diode characteristics. Figure 2 shows the $I-V$ of the as-grown ("unannealed") junction, as well as that of a junction capped and annealed at 750 °C for 1 h. The two $I-V$s appear to be identical, suggesting that the elevated temperature alone has a negligible effect on diode character-

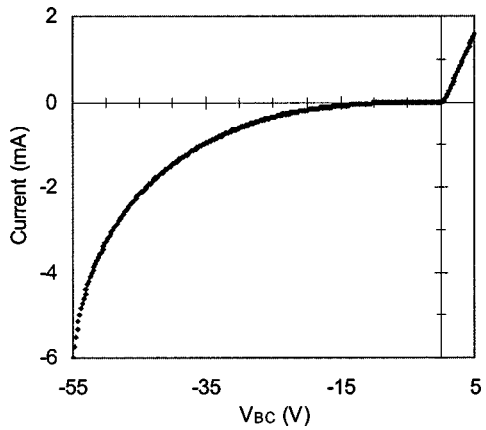

FIG. 1. Room-temperature $I-V$ characteristic for the *p*-GaAs/*n*-GaN base-collector junction, fabricated via wafer fusion at 750 °C for 1 h.

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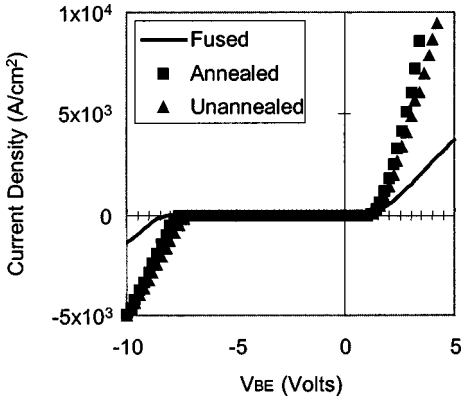

FIG. 2. Room-temperature $I-V$ characteristic for the *p*-GaAs/*n*-AlGaAs diode, subjected to three different process conditions: as grown by MBE (unannealed), capped and annealed at 750 °C for 1 h, and fused at 750 °C for 1 h to an *n*-GaN collector.

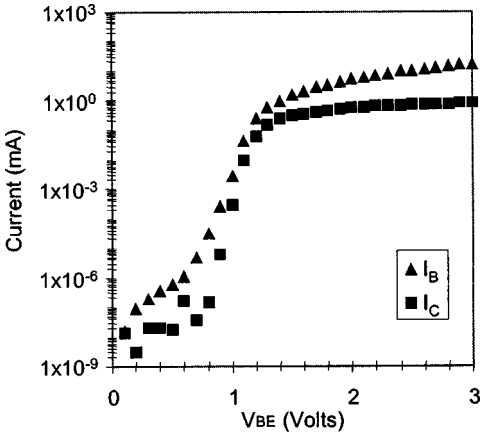

FIG. 4. Room-temperature Gummel plot for the *n*-AlGaAs/*p*-GaAs/*n*-GaN HBT.

istics. However, the $I-V$ appears to degrade for a diode fused to GaN under those same conditions (750 °C for 1 h). As seen in studies of GaAs–InP wafer-fused interfaces, disorder at the fused interface can produce enhanced diffusion of defects and dopants under elevated temperature.[9] Future work will investigate if reduced fusion temperatures mitigate this effect. Despite the addition of a series resistance, the $I-V$ of the fused diode is similar to that of the unannealed and annealed diodes: all three exhibit $n\sim 1.2-1.5$, similar turn-on, low leakage current, and similar breakdown.

Figures 3 and 4 display the common-emitter characteristic and Gummel plot. The output current density is a modest but encouraging $\sim$100 A/cm^2. The low V_{CE} offset (1 V) indicates low parasitic resistance. The offset can be further decreased by annealing the base contacts. Most prominently, the current gain (β) is less than one, and it is important to understand the major limitations of β. Under the conditions that the emitter injection coefficient is nearly ideal ($\sim$1), β would have the following dependence:

$$\beta = 2D_{nB}\tau_{nB}/W_B^2,$$

where D_{nB} is the minority carrier (electron) diffusivity constant in the base, τ_{nB} is the minority carrier lifetime in the base, and W_B is the width of the base (0.15 μm). Since the emitter-base junction is a MBE-grown AlGaAs–GaAs heterostructure, we would expect to exhibit values of β comparable to those demonstrated in AlGaAs–GaAs HBTs ($\beta \sim 20-100$ for similar emitter-base structures and device sizes).[10,11] Our earlier studies have shown that wafer fusion at elevated temperatures promotes the diffusion of dopants across interfaces (to be published elsewhere). This ''cross diffusion'' could in turn reduce both τ_{nB} and D_{nB}, leading to a reduced value of β. Our work with wafer-fused GaAs–GaN diodes has shown that mechanically and electronically stable junctions can be obtained for fusion temperatures as low as 500 °C. Lower temperatures would mitigate such diffusion effects. In addition, uncontrolled bond reconstruction or residual impurities at the fused interface can produce electronic traps, which could also limit β. Moreover, the true GaAs–GaN conduction band gap offset is unknown. McCarthy *et al.*[12] calculated offsets in the conduction band (ΔE_C) and valence band (ΔE_V) of -0.1 and -2.1 eV, using values of electron affinity for GaAs (4.07 eV) and GaN (4.2 eV), and not accounting for interface states. If ΔE_C were $+0.1$ eV (or less), rather than -0.1 eV, that spike in the conduction band could lead to a substantial reduction in collector current, and hence current gain. Future work will examine the effect of placing the fused interface slightly into the collector region, away from the actual base-collector junction.

This study demonstrated the AlGaAs–GaAs–GaN HBT, in which the lattice-mismatched GaAs–GaN junction was achieved via wafer fusion. The devices displayed low V_{CE} offset, with a less-than-unity common-emitter current gain. The initial characterization of the fused HBT provides important insights that suggest improvements in future devices. Wafer fusion at lower temperatures, and setting the fused interface slightly away from the exact base-collector junction, may improve HBT parameters such as the current gain.

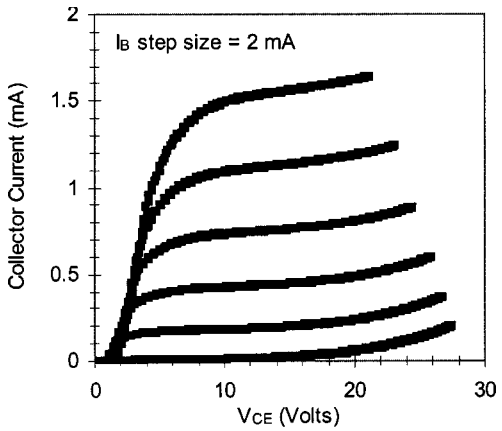

FIG. 3. Room-temperature common-emitter characteristic for the *n*-AlGaAs/*p*-GaAs/*n*-GaN HBT.

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